3.3 V ECL 8-Bit Synchronous Binary Up Counter

MC100EP016A

Description

The MC100EP016A is a high−speed synchronous, presettable, cascadeable 8−bit binary counter. Architecture and operation are the same as the ECLinPS™ family MC100E016 with higher operating speed.

The counter features internal feedback to $\overline{TC}$ gated by the TCLD (Terminal Count Load) pin. When TCLD is LOW (or left open, in which case it is pulled LOW by the internal pulldowns), the $\overline{TC}$ feedback is disabled, and counting proceeds continuously, with $\overline{TC}$ going LOW to indicate an all−one state. When TCLD is HIGH, the TC feedback causes the counter to automatically reload upon TC = LOW, thus functioning as a programmable counter. The Qn outputs do not need to be terminated for the count function to operate properly. To minimize noise and power, unused Q outputs should be left unterminated.

COUT and $\overline{COUT}$ provide differential outputs from a single, non−cascaded counter or divider application. COUT and $\overline{COUT}$ should not be used in cascade configuration. Only $\overline{TC}$ should be used for a counter or divider cascade chain output.

A differential clock input has also been added to improve performance.

The 100 Series contains temperature compensation.

Features

- 550 ps Typical Propagation Delay
- Operation Frequency > 1.3 GHz is 30% Faster than MC100EP016
- PECL Mode Operating Range: V_{CC} = 3.0 V to 3.6 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = −3.0 V to −3.6 V
- Open Input Default State
- Safety Clamp on Clock Inputs
- Internal $\overline{TC}$ Feedback (Gated)
- Addition of COUT and $\overline{COUT}$
- 8−Bit
- Differential Clock Input
- V_{BB} Output
- Fully Synchronous Counting and $\overline{TC}$ Generation
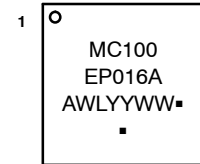- Asynchronous Master Reset
- Pb−Free Packages are Available

MARKING DIAGRAMS*

**LQFP−32, 7x7
CASE 561AB**

MC100
EP016A
AWLYYWWG
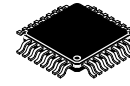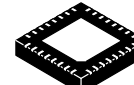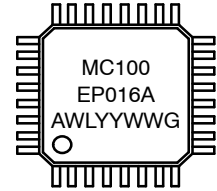
**QFN32
MN SUFFIX
CASE 488AM**

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MC100
EP016A
AWLYYWW■
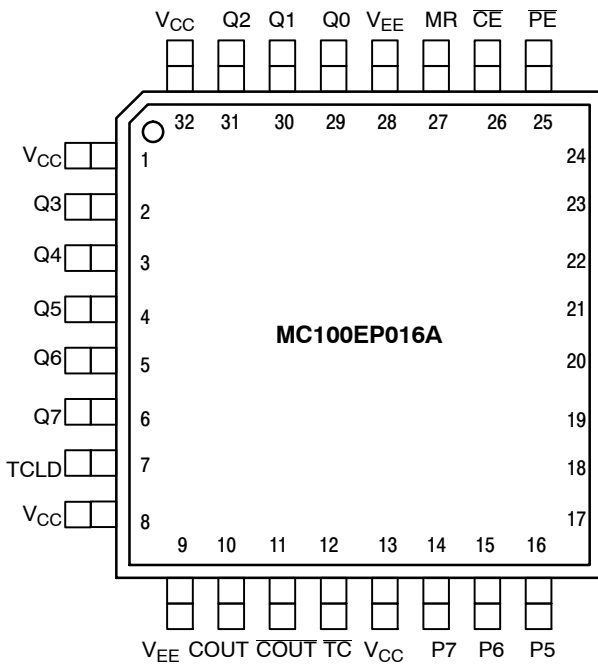■

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G or ■ = Pb−Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

MC100EP016A

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

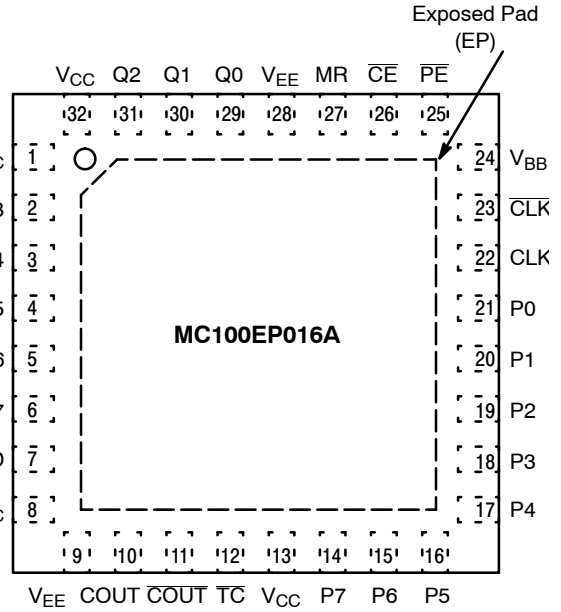**Figure 1. 32−Lead LQFP Pinout** (Top View)

Figure 2. 32−Lead QFN Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Function
P0–P7	ECL Parallel Data (Preset) Inputs
Q0–Q7	ECL Data Outputs
$\overline{CE}$*	ECL Count Enable Control Input
$\overline{PE}$*	ECL Parallel Load Enable Control Input
MR*	ECL Master Reset
CLK*, $\overline{CLK}$*	ECL Differential Clock
$\overline{TC}$	ECL Terminal Count Output
TCLD*	ECL TC−Load Control Input
COUT, $\overline{COUT}$	ECL Differential Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
V_{BB}	Reference Voltage Output
EP	The exposed pad (EP) on the QFN−32 package bottom is thermally connected to the die for improved heat−sinking conduit. The pad is electrically connected to V_{EE}.

*Pins will default LOW when left open.

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Table 2. FUNCTION TABLE

$\overline{CE}$	$\overline{PE}$	TCLD	MR	CLK	FUNCTION
X	L	X	L	Z	Load Parallel (Pn to Qn)
L	H	L	L	Z	Continuous Count
L	H	H	L	Z	Count; Load Parallel on $\overline{TC}$ = LOW
H	H	X	L	Z	Hold
X	X	X	L	ZZ	Masters Respond, Slaves Hold
X	X	X	H	X	Reset (Qn : = LOW, $\overline{TC}$: = HIGH)

ZZ = Clock Pulse (High–to–Low)
Z = Clock Pulse (Low–to–High)

Table 3. FUNCTION TABLE

Function	PE	CE	MR	TCLD	CLK	P7–P4	P3	P2	P1	P0	Q7–Q4	Q3	Q2	Q1	Q0	$\overline{TC}$	$\overline{COUT}$	COUT
Load Count	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H	H	L
	H	L	L	L	Z	X	X	X	X	X	H	H	H	L	H	H	H	L
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	L	H	H	L
	H	L	L	L	Z	X	X	X	X	X	H	H	H	H	H	L	L	H
	H	L	L	L	Z	X	X	X	X	X	L	L	L	L	L	H	H	L
Load Hold	L	X	L	X	Z	H	H	H	L	L	H	H	H	L	L	H	H	L
	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H	H	L
	H	H	L	X	Z	X	X	X	X	X	H	H	H	L	L	H	H	L
Load on Terminal Count	H	L	L	H	Z	H	L	H	H	L	H	H	H	L	H	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	L	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	H	H	H	H	L	L	H
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	L	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	L	H	H	H	H	H	L
	H	L	L	H	Z	H	L	H	H	L	H	H	L	L	L	H	H	L
Reset	X	X	H	X	X	X	X	X	X	X	L	L	L	L	L	H	H	L

MC100EP016A
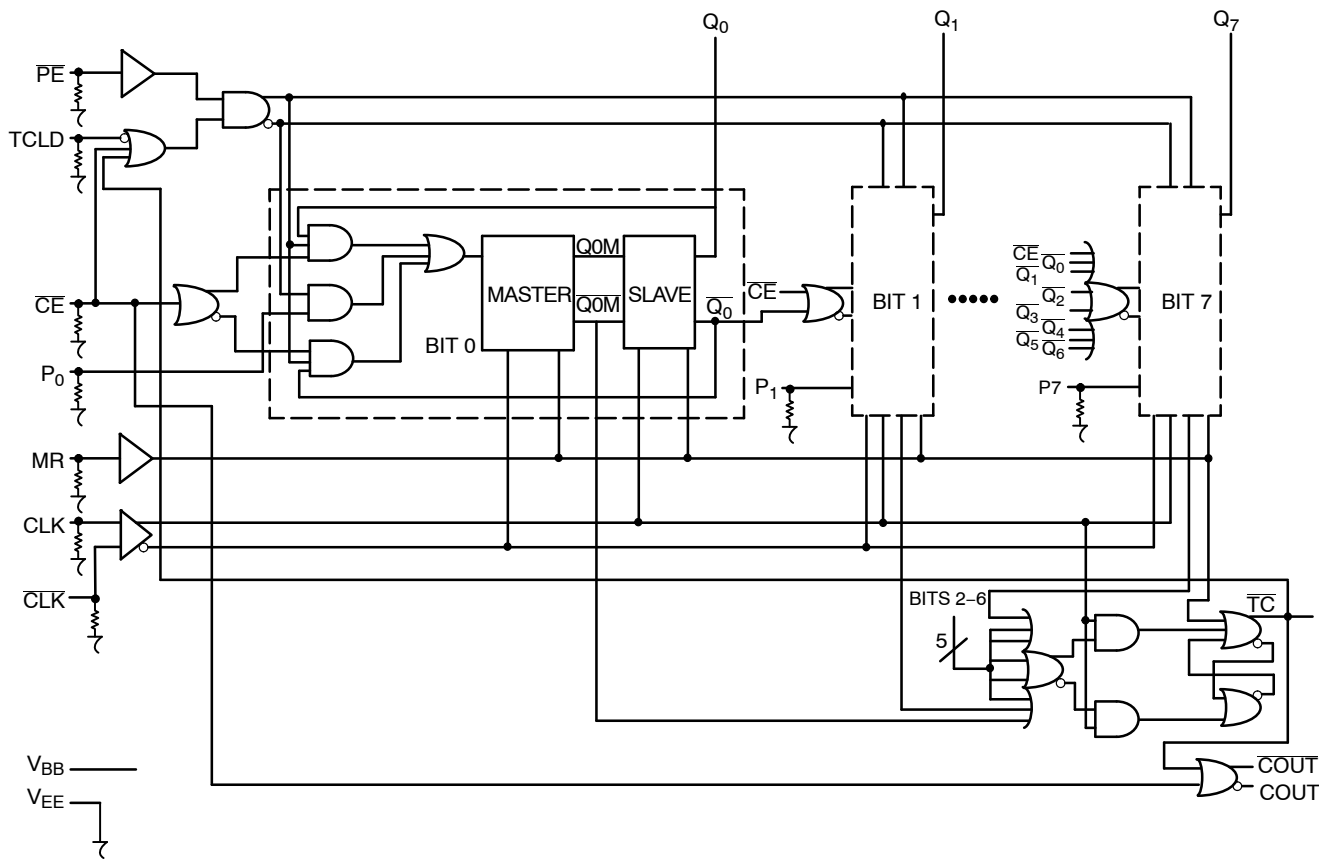
Note that this diagram is provided for understanding of logic operation only.
It should not be used for propagation delays as many gate functions are achieved internally without incurring a full gate delay.

Figure 3. 8-BIT Binary Counter Logic Diagram

Table 4. ATTRIBUTES

Characteristics		Value	
Internal Input Pulldown Resistor		75 kΩ	
Internal Input Pullup Resistor		N/A	
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 100 V > 2 kV	
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Pb Pkg	Pb−Free Pkg
	LQFP−32 QFN−32	Level 2 N/A	Level 2 Level 1
Flammability Rating Oxygen Index: 28 to 34		UL 94 V−0 @ 0.125 in	
Transistor Count		1226 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

1. For additional information, see Application Note AND8003/D.

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	$V_{EE} = 0$ V		6	V
V_{EE}	NECL Mode Power Supply	$V_{CC} = 0$ V		−6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0$ V $V_{CC} = 0$ V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 −6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			−40 to +70	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	32 LQFP 32 LQFP	74 61	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	32 LQFP	12 to 17	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	QFN−32 QFN−32	31 27	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P	QFN−32	12	°C/W
T_{sol}	Wave Solder Pb Pb−Free			265 265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 6. 100EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 2)

Symbol	Characteristic	−40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	130	170	210	130	177	210	130	180	210	mA
V_{OH}	Output HIGH Voltage (Note 3)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 3)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single−Ended)	1355		1675	1355		1675	1355		1675	mV
V_{BB}	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to −0.3 V.
3. All loading with 50 ohms to V_{CC}−2.0 volts.
4. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

Table 7. 100EP DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = −3.6 V to −3.0 V (Note 5)

Symbol	Characteristic	−40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	130	170	210	130	177	210	130	180	210	mA
V_{OH}	Output HIGH Voltage (Note 6)	−1145	−1020	−895	−1145	−1020	−895	−1145	−1020	−895	mV
V_{OL}	Output LOW Voltage (Note 6)	−1945	−1820	−1695	−1945	−1820	−1695	−1945	−1820	−1695	mV
V_{IH}	Input HIGH Voltage (Single−Ended)	−1225		−880	−1225		−880	−1225		−880	mV
V_{IL}	Input LOW Voltage (Single−Ended)	−1945		−1625	−1945		−1625	−1945		−1625	mV
V_{BB}	Output Voltage Reference	−1525	−1425	−1325	−1525	−1425	−1325	−1525	−1425	−1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Input and output parameters vary 1:1 with V_{CC}.
6. All loading with 50 ohms to V_{CC}−2.0 volts.
7. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

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Table 8. AC CHARACTERISTICS V_{EE} = −3.0 V to −3.6 V; V_{CC} = 0 V or V_{CC} = 3.0 V to 3.6 V; V_{EE} = 0 V (Note 8)

Symbol	Characteristic		−40°C			25°C			70°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{COUNT}	Maximum Frequency Count & Division Modes Q, $\overline{TC}$, COUT/$\overline{COUT}$		1.3	1.5		1.2	1.4		1.2	1.3		GHz
t_{PLH} t_{PHL}	Propagation Delay	CLK to Q	350	511	650	400	550	700	480	610	780	ps
		MR to Q	400	550	700	400	570	750	450	630	820	
		CLK to $\overline{TC}$	350	511	650	400	550	700	480	610	780	
		MR to $\overline{TC}$	400	555	700	400	570	750	520	635	820	
		CLK to COUT/$\overline{COUT}$	475	705	850	500	745	900	550	825	1000	
		MR to COUT/$\overline{COUT}$	450	720	850	500	760	900	570	830	950	
t_S	Setup Time	P0	400	240		400	240		400	245		ps
		P1 to P4	300	140		300	135		300	125		
		P5 to P7	250	80		250	65		250	55		
		$\overline{CE}$	500	320		500	330		500	340		
		$\overline{PE}$	500	315		500	320		500	325		
		TCLD	550	355		550	365		550	380		
t_H	Hold Time	P0	100	−145		100	−155		100	−170		ps
		P1 to P4	50	−160		50	−170		50	−180		
		P5 to P7	150	−105		150	−110		150	−115		
		$\overline{CE}$	600	380		600	410		600	450		
		$\overline{PE}$	625	465		625	500		625	535		
		TCLD	525	320		525	325		525	340		
t_{JITTER}	Clock Random Jitter (RMS, 1000 Waveforms)			2.6	8.5		2.5	8.0		2.5	8.0	ps
t_{RR}	Reset Recovery Time		400	195		400	205		400	220		ps
t_{PW}	Minimum Pulse Width CLK Minimum Pulse Width MR		385 550	334 380		416 550	357 380		416 550	385 380		ps
t_r, t_f	Output Rise/Fall Times 20% − 80%		90	180	320	100	190	320	125	215	450	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to V_{CC}−2.0 V.

APPLICATIONS INFORMATION

Cascading Multiple EP016A Devices

   For applications which call for larger than 8-bit counters multiple EP016As can be tied together to achieve very wide bit width counters. The active low terminal count ($\overline{TC}$) output and count enable input ($\overline{CE}$) greatly facilitate the cascading of EP016A devices. Two EP016As can be cascaded without the need for external gating, however for counters wider than 16 bits external OR gates are necessary for cascade implementations.

   Figure 4 below pictorially illustrates the cascading of 4 EP016As to build a 32-bit high frequency counter. Note the EP01 gates used to OR the terminal count outputs of the lower order EP016As to control the counting operation of the higher order bits. When the terminal count of the preceding device (or devices) goes low (the counter reaches an all 1s state) the more significant EP016A is set in its count mode and will count one binary digit upon the next positive clock transition. In addition, the preceding devices will also

count one bit thus sending their terminal count outputs back to a high state disabling the count operation of the more significant counters and placing them back into hold modes. Therefore, for an EP016A in the chain to count, all of the lower order terminal count outputs must be in the low state. The bit width of the counter can be increased or decreased by simply adding or subtracting EP016A devices from Figure 4 and maintaining the logic pattern illustrated in the same figure.

   The maximum frequency of operation for a cascaded counter chain is set by the propagation delay of the $\overline{TC}$ output, the necessary setup time of the $\overline{CE}$ input, and the propagation delay through the OR gate controlling it (for 16–bit counters the limitation is only the $\overline{TC}$ propagation delay and the $\overline{CE}$ setup time). Figure 4 shows EP01 gates used to control the count enable inputs, however, if the frequency of operation is slow enough, a LVECL OR gate can be used. Using the worst case guarantees for these parameters.
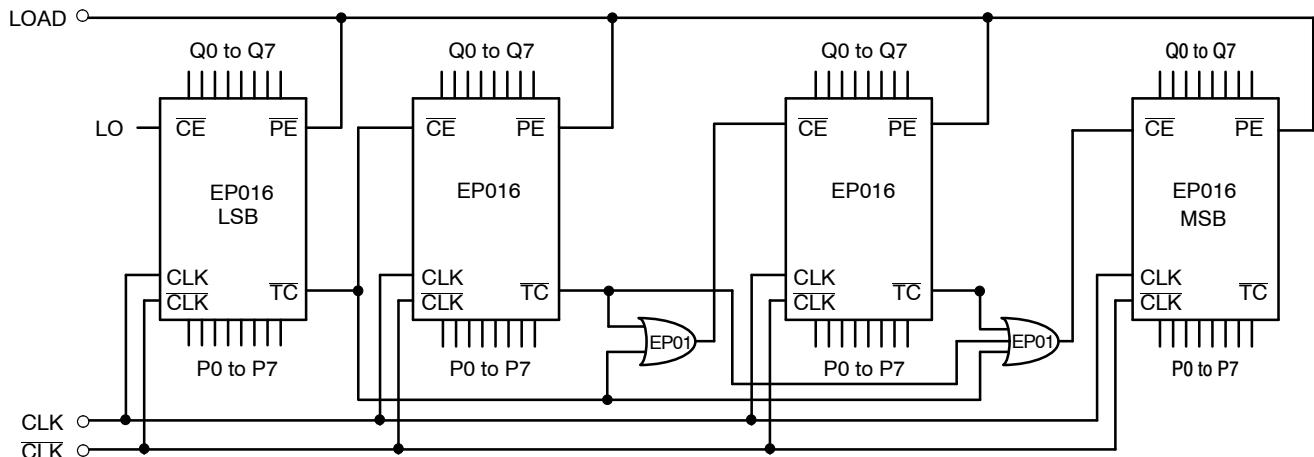
Figure 4. 32-Bit Cascaded EP016A Counter

   Note that this assumes the trace delay between the $\overline{TC}$ outputs and the $\overline{CE}$ inputs are negligible. If this is not the case estimates of these delays need to be added to the calculations.

Programmable Divider

   The EP016A has been designed with a control pin which makes it ideal for use as an 8-bit programmable divider. The TCLD pin (load on terminal count) when asserted reloads the

data present at the parallel input pin (Pn's) upon reaching terminal count (an all 1s state on the outputs). Because this feedback is built internal to the chip, the programmable division operation will run at very nearly the same frequency as the maximum counting frequency of the device. Figure 5 below illustrates the input conditions necessary for utilizing the EP016A as a programmable divider set up to divide by 113.

APPLICATIONS INFORMATION (continued)
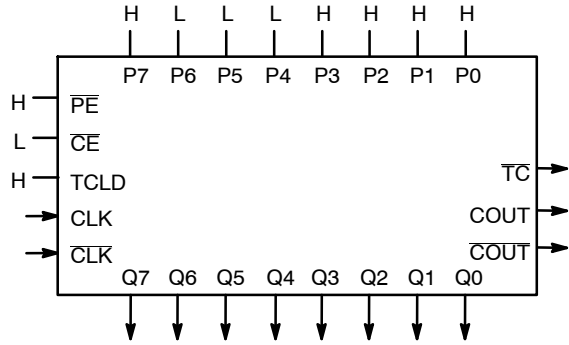
Figure 5. Mod 2 to 256 Programmable Divider

To determine what value to load into the device to accomplish the desired division, the designer simply subtracts the binary equivalent of the desired divide ratio from the binary value for 256. As an example for a divide ratio of 113:

Pn's = $256 - 113 = 8F_{16} = 1000\ 1111$

where:

P0 = LSB and P7 = MSB

Forcing this input condition as per the setup in Figure 5 will result in the waveforms of Figure 6. Note that the $\overline{TC}$ output is used as the divide output and the pulse duration is equal to a full clock period. For even divide ratios, twice the desired divide ratio can be loaded into the EP016A and the $\overline{TC}$ output can feed the clock input of a toggle flip flop to create a signal divided as desired with a 50% duty cycle.

Table 9. Preset Values for Various Divide Ratios

Divide Ratio	Preset Data Inputs							
	P7	P6	P5	P4	P3	P2	P1	P0
2	H	H	H	H	H	H	H	L
3	H	H	H	H	H	H	L	H
4	H	H	H	H	H	H	L	L
5	H	H	H	H	H	L	H	H
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
112	H	L	L	H	L	L	L	L
113	H	L	L	L	H	H	H	H
114	H	L	L	L	H	H	H	L
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
254	L	L	L	L	L	L	H	L
255	L	L	L	L	L	L	L	H
256	L	L	L	L	L	L	L	L

A single EP016A can be used to divide by any ratio from 2 to 256 inclusive. If divide ratios of greater than 256 are needed multiple EP016As can be cascaded in a manner similar to that already discussed. When EP016As are cascaded to build larger dividers the TCLD pin will no longer provide a means for loading on terminal count. Because one does not want to reload the counters until all of the devices in the chain have reached terminal count, external gating of the $\overline{TC}$ pins must be used for multiple EP016A divider chains.
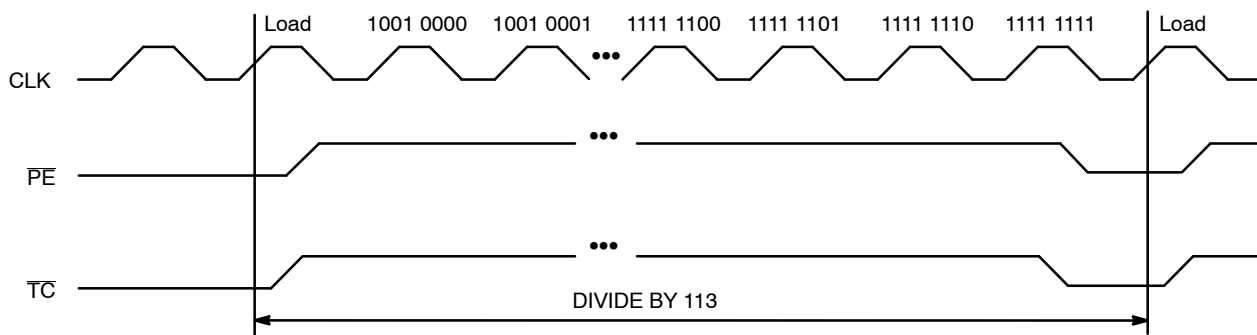
Figure 6. Divide by 113 EP016A Programmable Divider Waveforms

APPLICATIONS INFORMATION (continued)
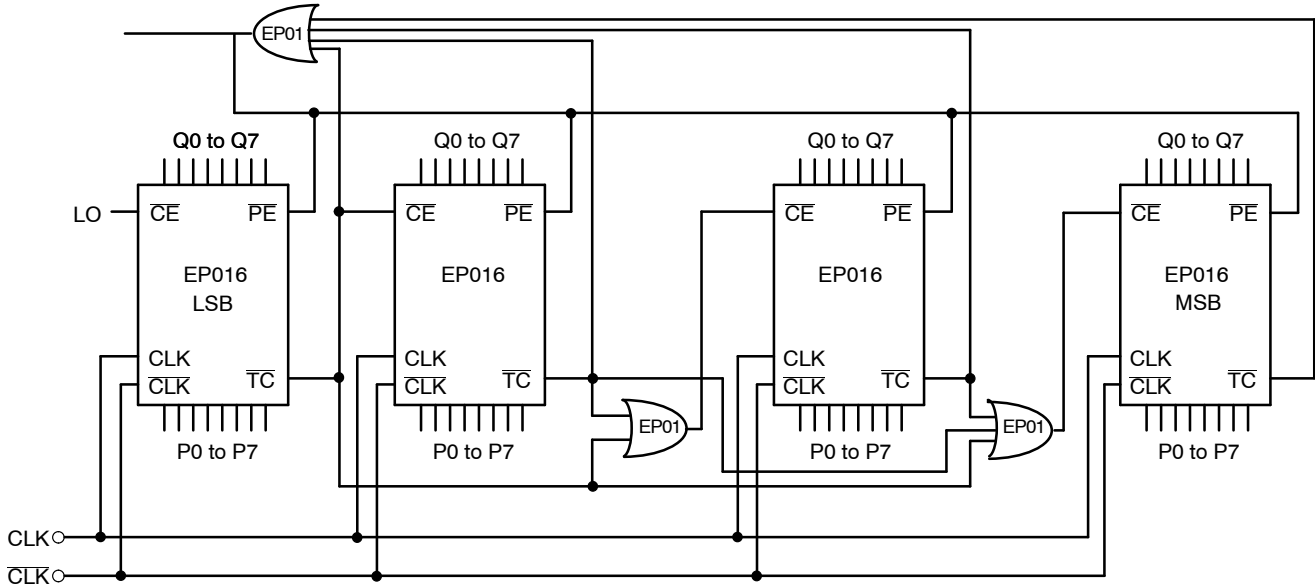
Figure 7. 32-Bit Cascaded EP016A Programmable Divider

Figure 7 shows a typical block diagram of a 32-bit divider chain. Once again to maximize the frequency of operation EP01 OR gates were used. For lower frequency applications a slower OR gate could replace the EP01. Note that for a 16-bit divider the OR function feeding the $\overline{PE}$ (program enable) input CANNOT be replaced by a wire OR tie as the $\overline{TC}$ output of the least significant EP016A must also feed the $\overline{CE}$ input of the most significant EP016A. If the two $\overline{TC}$ outputs were OR tied the cascaded count operation would not operate properly. Because in the cascaded form the $\overline{PE}$ feedback is external and requires external gating, the maximum frequency of operation will be significantly less than the same operation in a single device.

Maximizing EP016A Count Frequency

The EP016A device produces 9 fast transitioning single ended outputs, thus V_{CC} noise can become significant in situations where all of the outputs switch simultaneously in the same direction. This V_{CC} noise can negatively impact the maximum frequency of operation of the device. Since the device does not need to have the Q outputs terminated to count properly, it is recommended that if the outputs are not going to be used in the rest of the system they should be left unterminated. In addition, if only a subset of the Q outputs are used in the system only those outputs should be terminated. Not terminating the unused outputs will not only cut down the V_{CC} noise generated but will also save in total system power dissipation. Following these guidelines will allow designers to either be more aggressive in their designs or provide them with an extra margin to the published data book specifications.
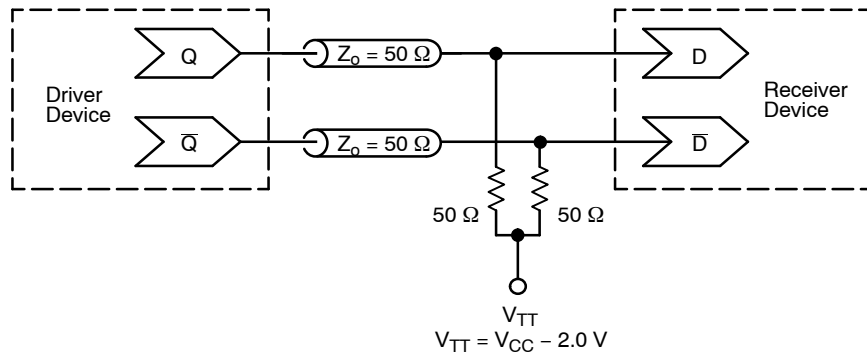
Figure 8. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

ORDERING INFORMATION

Device	Package	Shipping†
MC100EP016AFAG	LQFP−32 (Pb−Free)	250 Units / Tray
MC100EP016AMNG	QFN−32 (Pb−Free)	74 Units / Rail
MC100EP016AMNR4G	QFN−32 (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/**D** – ECL Clock Distribution Techniques

AN1406/**D** – Designing with PECL (ECL at +5.0 V)

AN1503/**D** – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/**D** – Metastability and the ECLinPS Family

AN1568/**D** – Interfacing Between LVDS and ECL

AN1672/**D** – The ECL Translator Guide

AND8001/**D** – Odd Number Counters Design

AND8002/**D** – Marking and Date Codes

AND8020/**D** – Termination of ECL Logic Devices

AND8066/**D** – Interfacing with ECLinPS

AND8090/**D** – AC Characteristics of ECL Devices
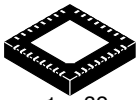
QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

DATE 23 OCT 2013

SCALE 2:1

1   32

PIN ONE LOCATION

0.15 | C

0.15 | C

TOP VIEW

0.10 | C   DETAIL B

0.08 | C

NOTE 4   **SIDE VIEW**

A
(A3)
A1

C SEATING PLANE

DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

L1   L   L

DETAIL A

EXPOSED Cu   MOLD CMPD

DETAIL B
ALTERNATE CONSTRUCTION

DETAIL A

D2   K

9

8   17

32X L

32X E2

1

32   25

32X b

e

e/2

0.10 M C A B
0.05 M C   NOTE 3

BOTTOM VIEW
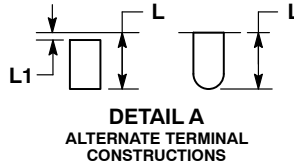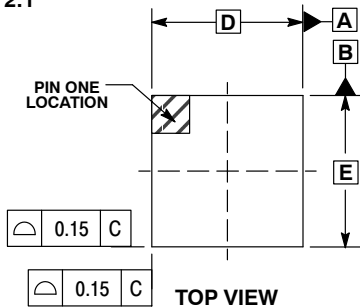
NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15
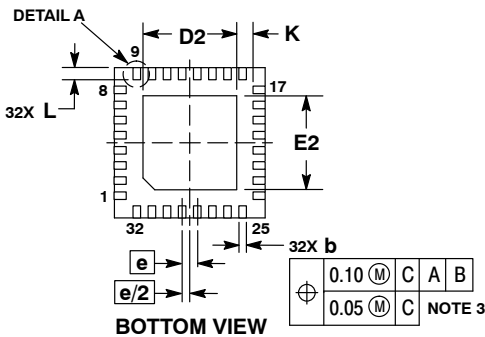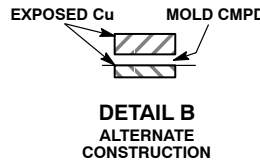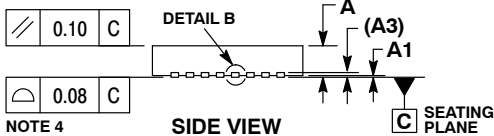
GENERIC MARKING DIAGRAM*

1   ○

XXXXXXXX
XXXXXXXX
AWLYYWW■

■
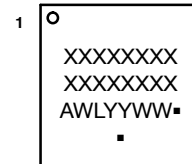
XXXXX   = Specific Device Code
A   = Assembly Location
WL   = Wafer Lot
YY   = Year
WW   = Work Week
■   = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb–Free indicator, "G" or microdot " ■", may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*

5.30
3.35
32X 0.63

3.35   5.30

0.50 PITCH
32X 0.30

DIMENSION: MILLIMETERS
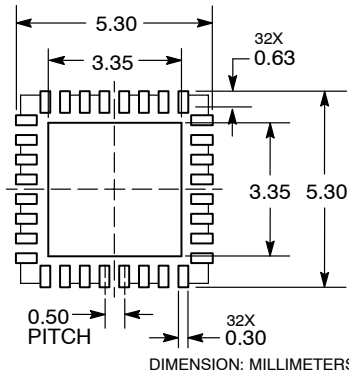
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	QFN32 5x5 0.5P	PAGE 1 OF 1

LQFP−32, 7x7
CASE 561AB
ISSUE O

DATE 19 JUN 2008

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
B	0.30	0.37	0.45
B1	0.30	0.35	0.40
C	0.09	–	0.20
C1	0.09	–	0.16
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.80 BSC.		
L	0.45	0.60	0.75
L1	1.00		
R1	0.08	–	0.20
$\alpha°$	11	–	13
$\beta°$	0	–	7
$\gamma°$	0	–	–

PIN 1 INDICATOR

SEE DETAIL A

SEE DETAIL B

DETAIL B

DETAIL A

R1 RADIUS
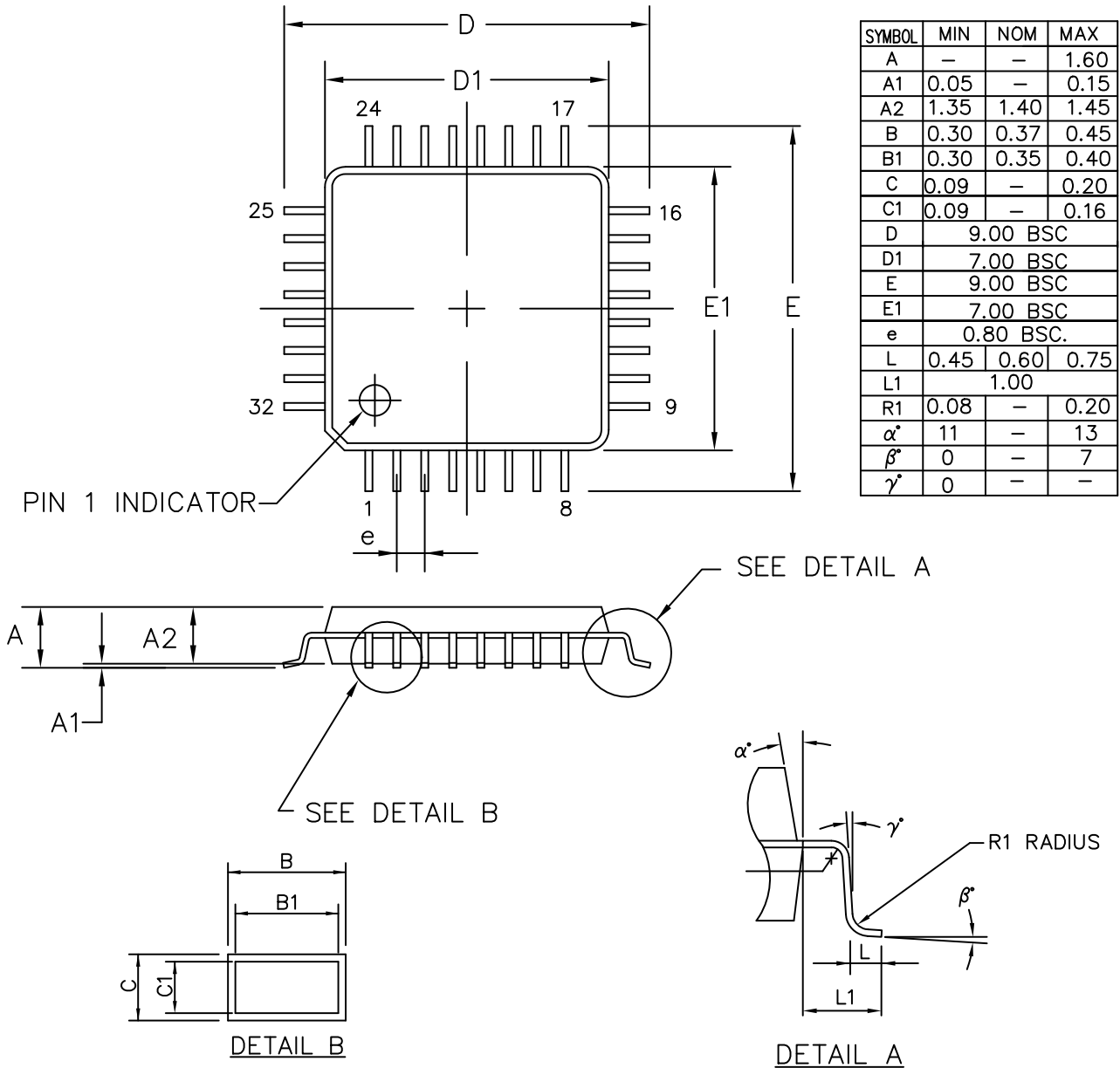
ALL DIMENSIONS IN MM

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DESCRIPTION:	**32 LEAD LQFP, 7X7**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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