Freescale Semiconductor
Technical Data

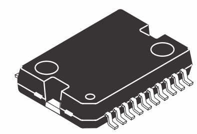
Document Number: MC33385
Rev. 6.0, 11/2006

Quad Low-side Driver

The MC33385 is a Quad Low-side Driver fully protected switch. This device is a general purpose Low-side Driver but has been especially designed to operate in engine management applications as injector driver or automotive gear box. It is interfaced directly with a microcontroller for parallel control of the load and the individual output diagnostic is done through a SPI. The diagnostic logic recognizes 4 failure types at each output stage: overcurrent, short to GND, open load, and over-temperature.

33385

LOW-SIDE DRIVER



DH SUFFIX
VW SUFFIX (PB-FREE)
98ASH70702A
20-PIN HSOP

Features

- RDSON of 250mΩ per Output at 25°C
- Supplied from the main 5V V_{CC}
- Input CMOS Compatible
- Diagnostic through SPI
- Nominal Current of 2A per Output
- Current Limitation at 3A with Automatic Turn Off
- Output Internally Clamped at 50V typ for Inductive Load Drive
- Junction to Case Thermal Resistance of 4.4°C/W
- Individual Output over Temperature Shutdown
- Pb-Free Packaging Designated by Suffix Code VW

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MC33385DH/R2	-40°C to 125°C	20 HSOP
MC33385VW/R2		

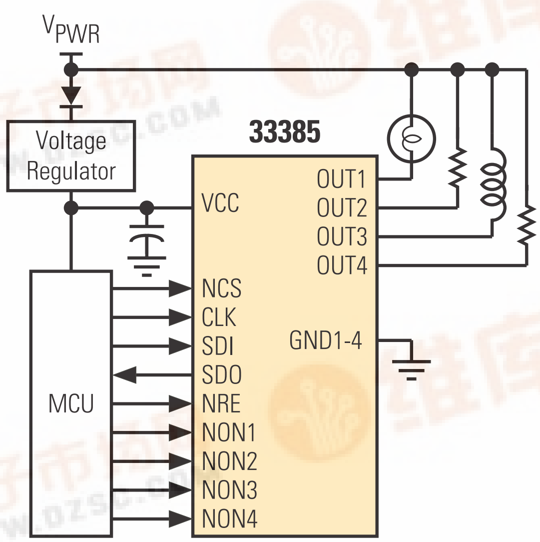


Figure 1. MC33385 Simplified Application Diagram

BLOCK DIAGRAM

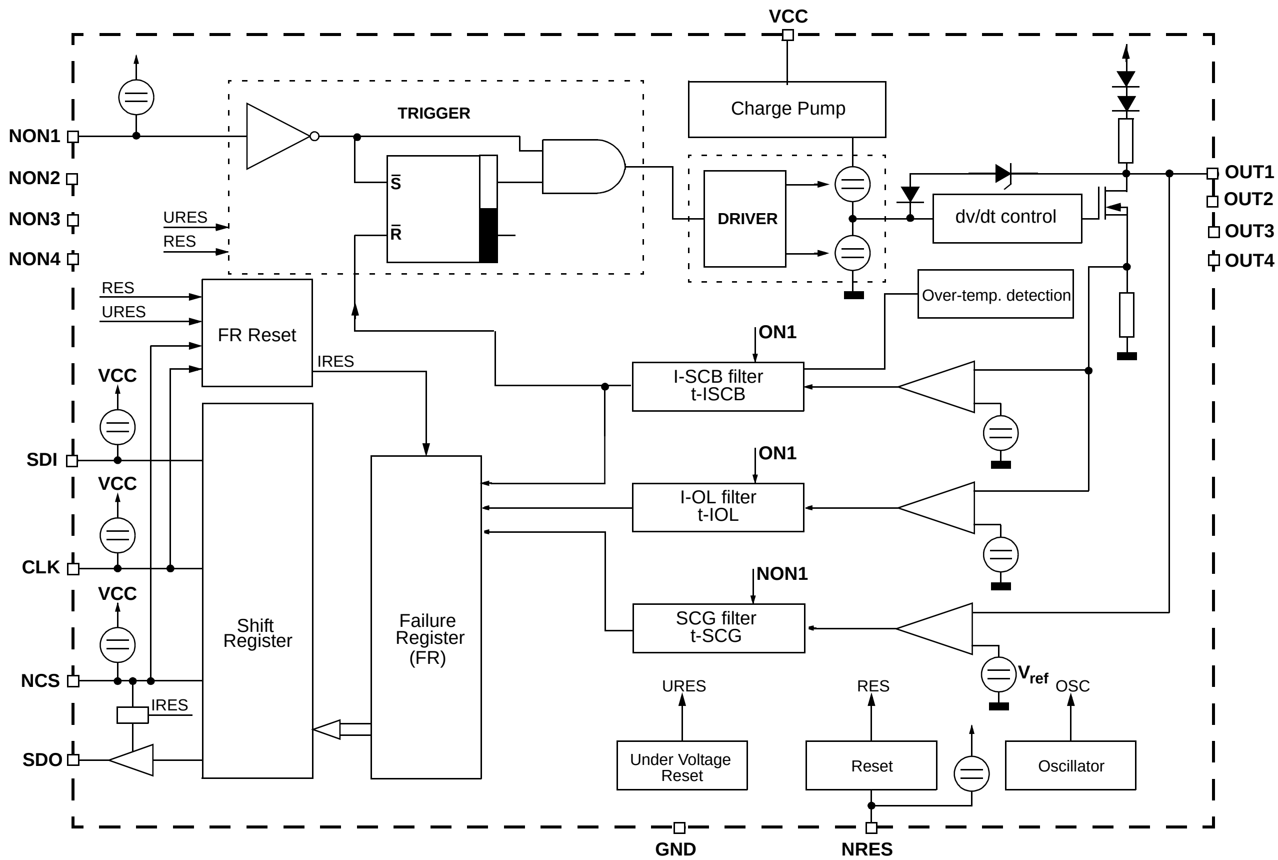


Figure 2. 33385 Simplified Internal Block Diagram

PIN CONNECTIONS

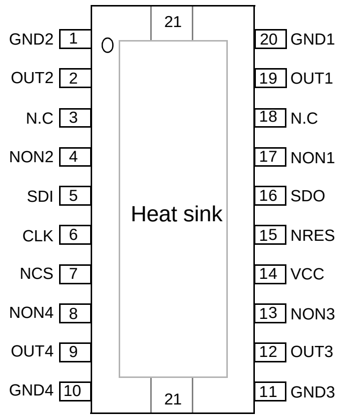


Figure 3. 33385 Pin Connections

Table 1. 33385 Pin Definitions

Pin Number	Pin Name	Definition
1	GND2	Ground 2
2	OUT2	Output Channel 2
3		NC
4	NON2	Input Control Signal for Channel 2
5	SDI	Serial Data Input
6	CLK	Clock Line for Serial Interface
7	NCS	Chip Select for Serial Interface
8	NON4	Input Control Signal for Channel 4
9	OUT4	Output Channel 4
10	GND4	Ground 4
11	GND3	Ground 3
12	OUT3	Output Channel 3
13	NON3	Input Control Signal for Channel 3
14	Vcc	5V Power Supply
15	NRES	Reset Input
16	SDO	Data Output of Serial Interface
17	NON1	Input Control Signal Channel 1
18		NC
19	OUT1	Output Channel 1
20	GND1	Ground 1
	Case	Connected to the PCB Ground for Thermal Purposes

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Voltage Range	Vcc	7.0	V
Continuous Output Voltage (With no reverse current)	V_{OUT}	45	V
Continuous Current	I_{OUTC}	2.5	A
Peak Output Current	I_{OUTP}	I_{SCBMAX}	A
Clamped Energy at the Switching OFF (See Figure 9)	W_{OFF}	70	mJ for 1ms
Input Voltage (Inputs)	V_{IN}	V_{CC} + 0.3	V
Input Protection Diode Current	I_{IN}	1.0	mA
Input Voltage (Outputs)	V_O	V_{CC} + 0.3	V
Input Protection Diode Current	I_O	1.0	mA
THERMAL RATINGS			
Operating Junction Temperature	T_J	150	°C
Thermal Resistance : Junction-case (One power stage in use)	R_{THJC}	4.5	kΩ
Thermal Resistance : Junction-ambient (Device soldered on printed circuit board)	R_{THJA}	50	kΩ
Peak Package Reflow Temperature During Reflow [(1)], [(2)]	T_{PPRT}	Note 2	°C

Notes
1. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
2. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

STATIC CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE					
Supply Voltage Range	V_{CC}	4.5		5.5	V
JUNCTION TEMPERATURE					
Junction Temperature Continuous (Continuous)	T_{J1}	- 40		150	°C
Junction Temperature Dynamical (Time limited)	T_{J2}			185	°C
OUTPUT CURRENT					
Output Current Range	I_{OUT}			I_{SCBMAX}	A
RESET BEHAVIOUR					
Reset Changeable (at NRES-Pin)	V_{CC}	V_{CCRES}		5.5	V
Undervoltage Reset (Independent of NRES) Active for V_{CC} = 0V to V_{CCPRO}	V_{CCRES}	3.35		3.95	V
UNDERVOLTAGE PROTECTION					
Protection active for V_{CC} =0V to V_{CCPRO}	V_{CCPRO}	1.5		4.0	V
OVER TEMPERATURE					
Temperature Detection Threshold	T_{OFF}	155		185	°C
SUPPLY CURRENT					
Standby Current (without load) (NON1...NON4 = High Level) 5.15V ≥ V_{CC} 5.5V ≥ V_{CC}	I_{CCSTB1} I_{CCSTB2}			6.0 7.0	mA mA
Operating Mode (For 5.15V ≥ V_{CC}) (Iout 1...4) = 2A	I_{CCOPM}			17	mA
ΔI_{CC} During Reverse Output Current (I_{OUT} = - 5A on one output)	ΔI_{CC}			100 50	mA mA
INPUTS (NONx, NCS, CLK, NRES, SDI)					
Low Threshold	V_{INL}	-0.3		0.2*V_{CC}	V
High Threshold	V_{INH}	0.7*V_{CC}		V_{CC} + 0.3	V
Hysteresis	V_{HYST}	0.85			V
Input Current (V_{IN} = V_{CC})	I_{IN}			10	µA
Input Current (V_{CC} >V_{RES} & 0V<V_{IN} < 0.9*V_{CC})	I_{IN}	- 100		- 20	µA
SERIAL DATA OUTPUT					
High Output Level (I_{SDO} = -2mA)	V_{SDOH}	V_{CC} - 0.4			V
Low Output Level (I_{SDO} = 3.2mA)	V_{SDOL}			0.4	V
Tristate Leakage Current (NCS = HIGH, V_{SDO} = 0V to V_{CC})	I_{SDOL}	- 10		10	µA
OUTPUTS (OUT 1...4)					
Average Output Current	I_{OUTA}	2.5			A
Output Peak Current	I_{OUTP}	I_{SCBMAX}			A

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40°C ≤ T_A ≤ 125°C, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Leakage Current 1 (NON = High, V_{OUT} = 25V, V_{CC} = 5V)	I_{OUTL}			10	µA
Leakage Current 2 (NON = High, V_{OUT} = 16V, V_{CC} = 1V)	I_{OUTL2}			10	µA
Output Clamp Voltage (I_{OUT} = 1A)	V_{CLP}	45	50	58	V
Matching Clamp Voltage (Between two outputs)	V_{CLPM}	V_{CLP-1}		V_{CLP+1}	V
Clamped Energy at the Switching OFF (See Figure 9)	W_{OFF}	50			mJ for 1ms
On Resistance (I_{OUT} = 2A, T_J = 150°C, NON = LOW)	R_{DSON}			500	mΩ
Output Low Voltage Limitation (I_{OUT} = 150mA)	V_{OUTLIM}	65		220	mV
Output Capacitance (Guaranteed by design)	C_{OUT}			350	pF
OUTPUTS REVERSE DIODE					
Reverse Output Current	I_{RD}	2,5			A
Reverse Peak current [1]	I_{RDP}	5.0			A
Reverse Voltage Drop - I_{OUT} = - 5A - I_{OUT} = - 2,5A	 V_{RD1} V_{RD2}	 1.0 0.85		 1.7 1.7	 V V
POWERSTAGE PROTECTION					
Short Current Limit	I_{SCB}	3.0		5	A
V_{CC} Undervoltage	V_{CCMIN}	3.35		3.95	V
DIAGNOSTIC					
Short to GND Threshold Voltage for I_{OUT} ≤ 2A	V_{REF}	0.390xV_{CC}		0.435xV_{CC}	V
Open Load Threshold Current	I_{OL}	10		50	mA
Pull-up Resistor	R_{OL}	2.0		8.0	kΩ
Temperature Detection Threshold	T_{OFF}	155		185	°C

Notes

1. For t ≤ 2ms. Max. reverse current is limited to - 10A (for all outputs together)

DYNAMIC CHARACTERISTIC

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions $7.0\ V \le V_{SUP} \le 18\ V$, $-40°C \le T_A \le 125°C$, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

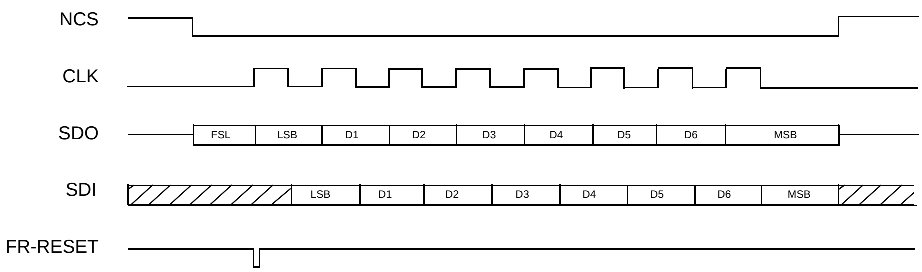
Characteristic	Symbol	Min	Typ	Max	Unit
INPUTS					
Input Frequency (NON1 to NON4)	f_{IN}	0.0		1000	Hz
OUTPUTS TIMING					
Positive Output Voltage Ramp (with inductive load) V_{OUT} = 4V... 16V V_{OUT} = 16V... Vclp	OVR_{P1} OVR_{P2}	2.0 3.5	3.0 6.0	5.0 10	V/µs V/µs
Negative Output Voltage Ramp (25%... 75%)	OVR_N	1.75	3.0	4.0	V/µs
Internal Switch-on-Time Charge Pump (NON = LOW... V_{GATE} = 0.9 * V_{BAT})	t_{DCP}			40	µs
Turn ON Delay (NON = 50%, V_{OUT} = 0.9 * V_{BAT})	t_{DON}	1.0	2.5	5.0	µs
Turn OFF Delay (NON = 50%, V_{OUT} = 0.1 * V_{BAT}) (NON = 50%, V_{OUT} = 4V)	t_{DOFFA} t_{DOFFB}		1.0 4.7	3.0 7.5	µs µs
Undervoltage Protection Max ON time after a output voltage ramp from 0V to 25V at V_{CC} = 0V...V_{CCPRO}	t_{RPON}			100	µs
Matching Turn ON Delay (NON = 50%, V_{OUT} = 0.9 * V_{BAT})	t_{MON}	- 3.0		3.0	µs
Rise time Turn OFF (10% - 90% of V_{CLP})	t_{ROFF}		8.5	12	µs
DIAGNOSTIC					
Short to GND Filter Time	T_{SCG}	140		250	µs
Open Load Filter Time	t_{OL}	140		250	µs
SERIAL DIAGNOSTIC LINK : LOAD CAPACITOR AT SDI AND SDO = 100PF					
Clock Frequency (50% duty cycle)	f_{CLK}	3.0			MHz
Minimum Time CLK = HIGH	t_{CLH}	100			ns
Minimum Time CLK = LOW	t_{CLL}	100			ns
Propagation Delay (CLF Data at SDO valid)	t_{PCLD}			100	ns
NCS = LOW to Data at SDO Valid	t_{PCLD}			100	ns
CLK Low Before NCS Low (Setup time CLK to NCS change High/Low)	t_{SCLCH}	100			ns
CLK Change Low/High after NCS = Low	t_{HCLCL}	100			ns
SDI Input Set up Time (CLK change High/Low after SDI data valid)	t_{SCLD}	20			ns
SDI Input Hold Time (SDI data hold after CLK change High/Low)	t_{HCLD}			20	ns
CLK Low Before NCS High	t_{SCLCL}	150			ns

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions $7.0\ V \le V_{SUP} \le 18\ V$, $-40°C \le T_A \le 125°C$, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25°C$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CLK High After NCS High	t_{HCLCH}	150			ns
NCSLow/High to Output Data Flout	t_{PCHDZ}			100	ns
Capacitance at SDI, SDO, CLk, CS	t_{PCLD}			10	pF
NCS Filter time (Pulses ≤ t_{FNCS} will be ignored)	t_{FNCS}	10		40	ns

TIMING DIAGRAMS



NOTE : FR -RESET means Reset failure storage (internal signal)

Figure 4. Timing Diagram to Read the Diagnostic Register

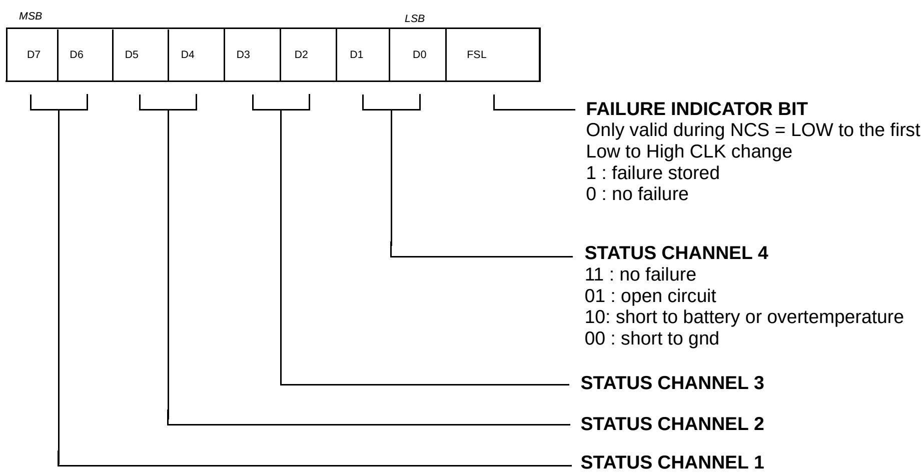


Figure 5. Diagnostic Failure Register Structure

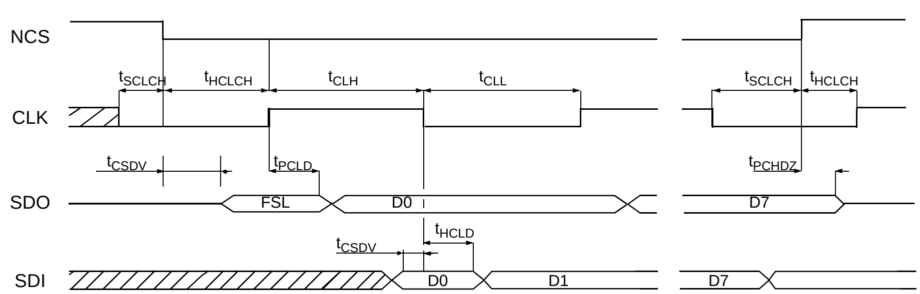


Figure 6. Serial Interface Timing

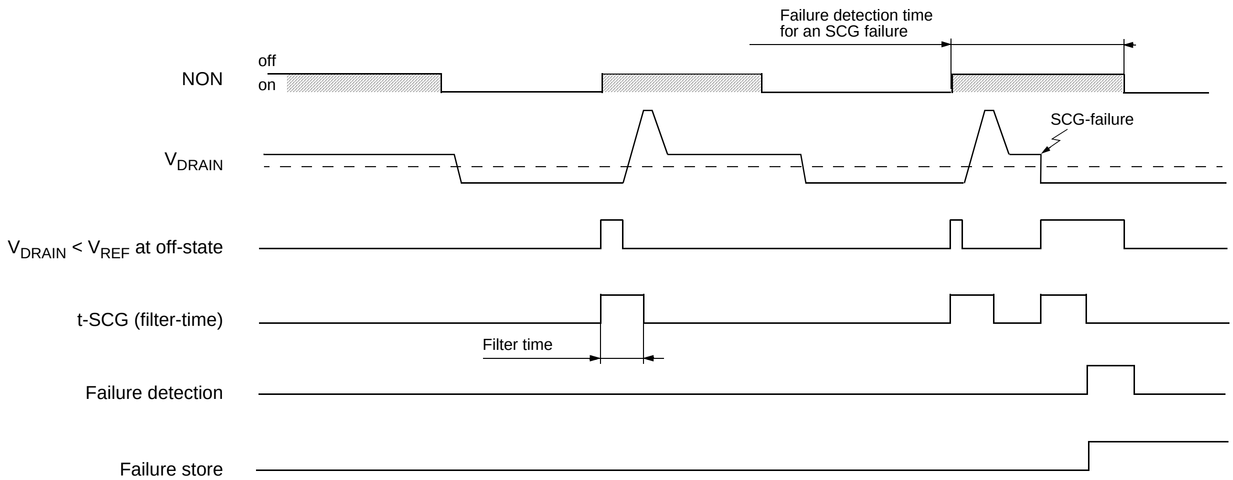


Figure 7. Diagram to Short-Circuit to GND Failure (SCG-Failure) Detection

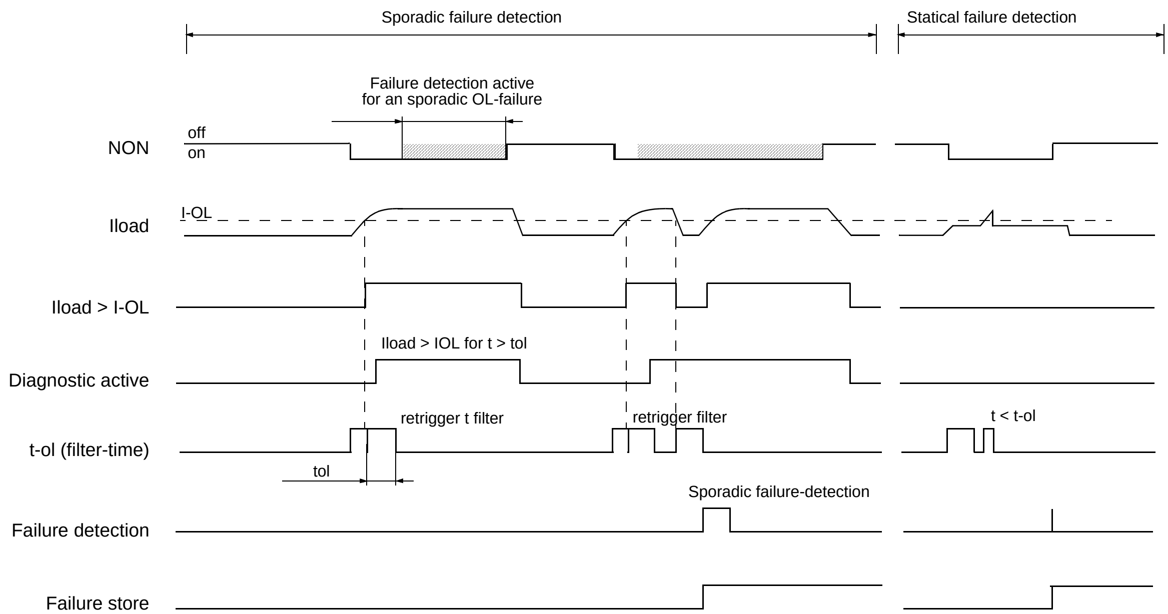


Figure 8. Diagram to Open Load Failure (OL-Failure) Detection

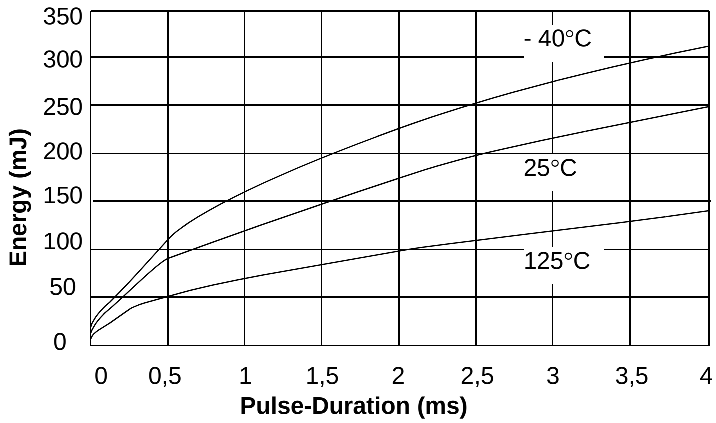


Figure 9. Max Clamp- Energy Specification

ELECTRICAL PERFORMANCE CURVES

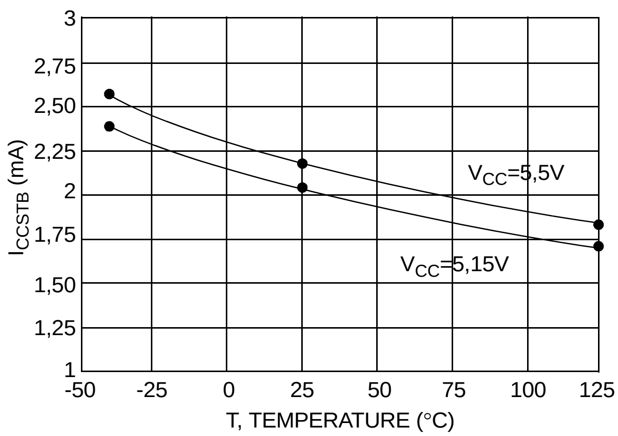


Figure 10. Standby Current versus Temperature

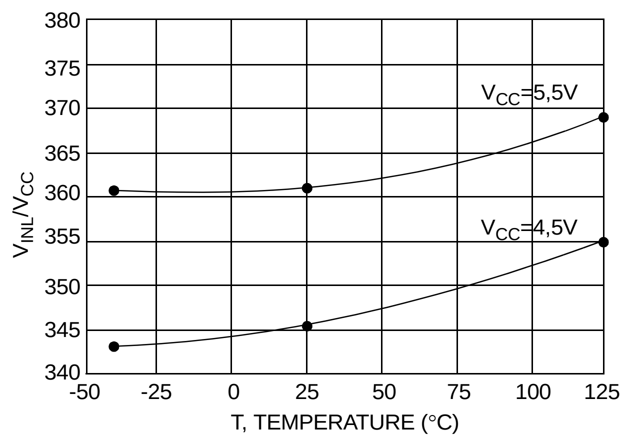


Figure 12. Low Threshold Input Voltage versus Temperature

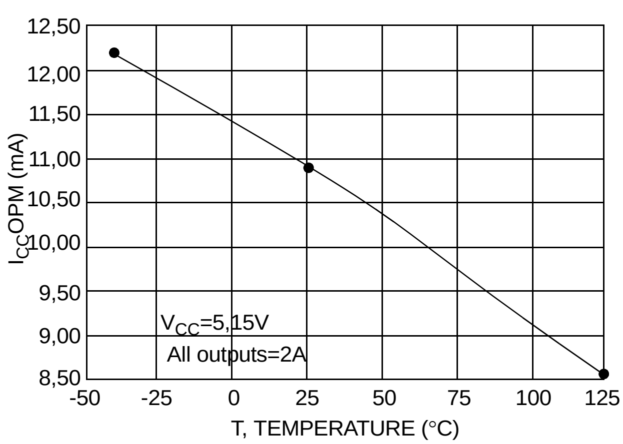


Figure 11. Operating Mode Current versus Temperature

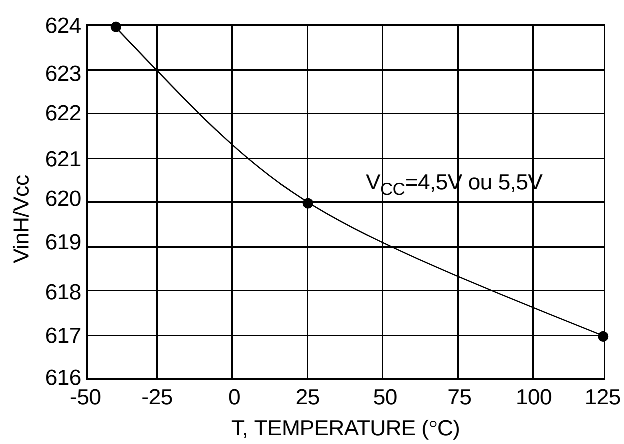


Figure 13. High Threshold Input Voltage versus Temperature

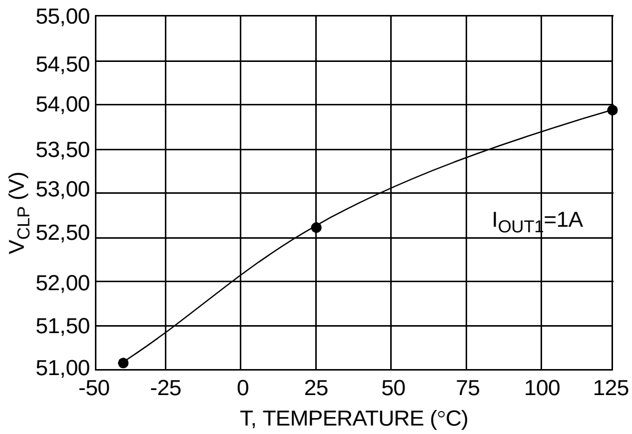


Figure 14. Output Clamp Voltage versus Temperature

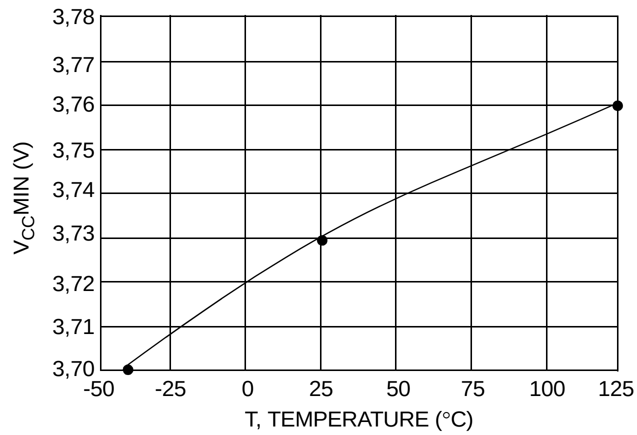


Figure 17. Vcc Undervoltage versus Temperature

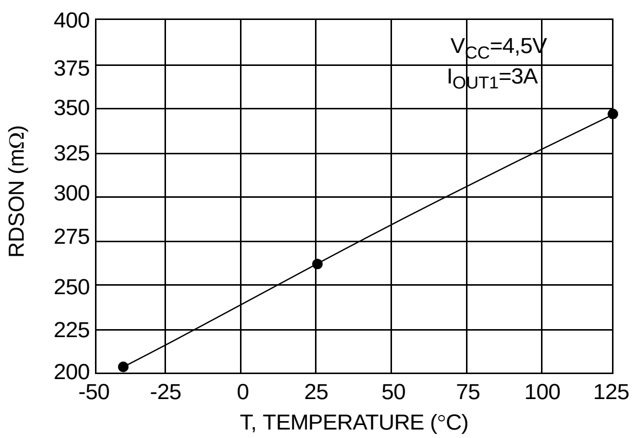


Figure 15. Rdson versus Temperature

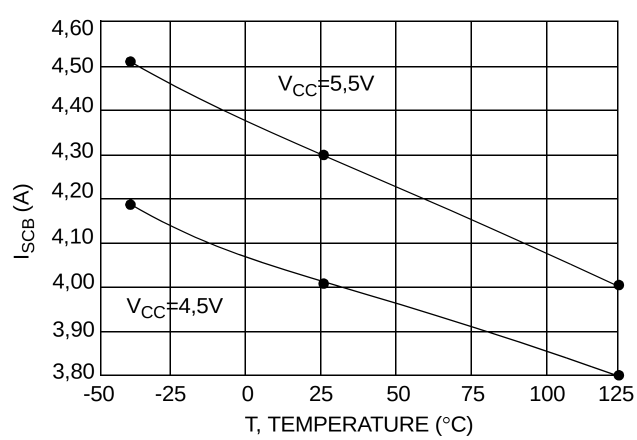


Figure 18. Short Current Limit versus Temperature

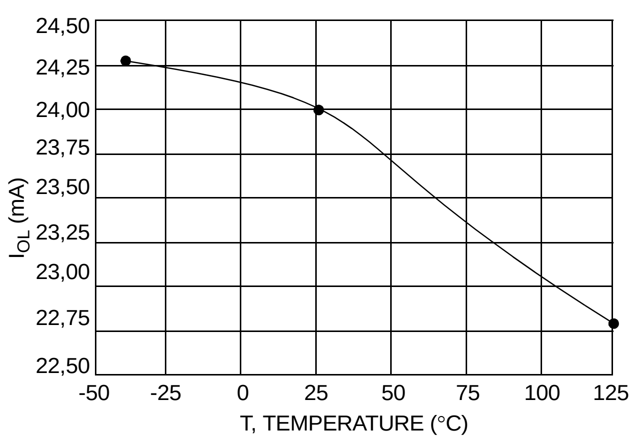


Figure 16. Open Load versus Temperature

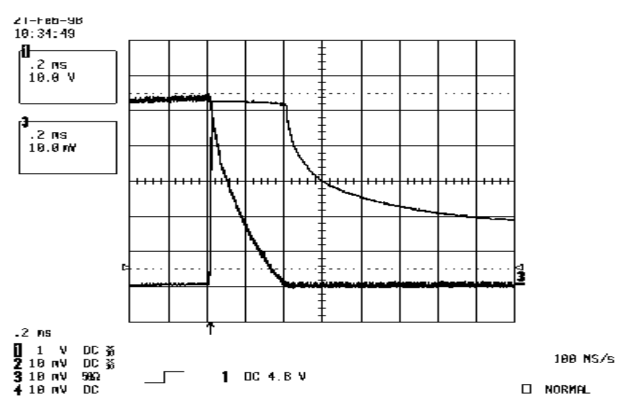


Figure 19. Inductive Switching

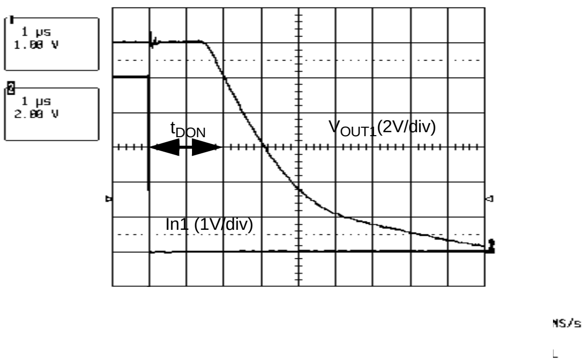


Figure 20. Turn on Delay

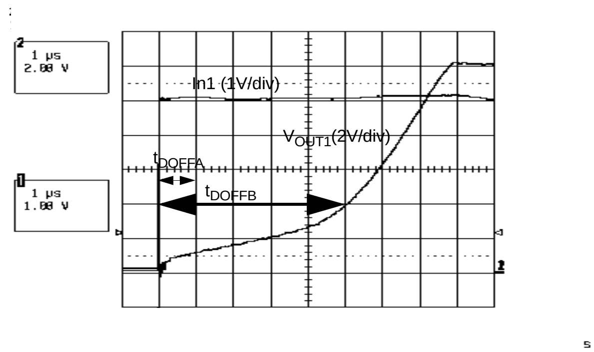


Figure 21. Turn off Delay

FUNCTIONAL DESCRIPTION

INTRODUCTION

The device is a Quad Low-side Driver driven by four CMOS input stages. Each output power transistor is protected against short to V_{BAT} by a zener clamp against overvoltage.

A diagnostic logic recognizes four failure types at the output stage : overcurrent, short to GND, open-load and overtemperature.

The failures are individually stored in a byte which can be read out via the serial interface (SPI).

OUTPUT STAGE CONTROL

Each of the four output stages is switched ON and OFF by an individual control line (NON-Input). The logic level of the control line is CMOS compatible. The output transistors are switched off when the inputs are not connected.

POWER TRANSISTORS

Each of the four output stages has its own zener clamp. This causes a voltage limitation at the power transistors when inductive loads are switched off. The drain voltage ramp occurring when output is switched on or off, is within defined limits. Output transistors can be connected in parallel to increase current capability. In this case, the associated inputs should be connected together.

SHORT-CIRCUIT AND OVERTEMPERATURE PROTECTION

If the output current increases above the short current limit for a time longer than t_{SCB} or if the temperature increases above T_{OFF} then the power transistor is immediately switched off. It remains switched off until the control signal on the NON-Input is switched off and on again.

DIAGNOSTICS

The following failures at the output stage are recognized :

Short -Circuit to V_{BAT} or overtemp = SCB (Highest priority)

Short -Circuit to GND................... = SCG

Open Load.................................... = OL (Lowest priority)

The SCB failure is recognized by an overcurrent (current above the short current limit) or an overtemperature.

If the current through the output stage is lower than the IOL-reference, after a filter time an OL failure will be recognized. This measurement is active while the power stage is switched on.

The SCG failure will recognize when the drain voltage is lower than the OL reference limit, while the output stage is switched off. All four outputs have an independent overtemperature detection and shutdown. All failures are stored in individual registers.

They can be read by the microprocessor via the serial interface. There is no failure detected if the power stage control time is shorter than the filter time.

DIAGNOSTIC INTERFACE

The communication between the microprocessor and the failure register runs via the SPI link. If there is a failure stored in the failure register, the first bit of the shift register is set to a high level. With the High/Low change on the NCS pin, the first bit of the diagnostic shift register will be transmitted to the SDO output. The SDO output is the serial output from the diagnostic shift register and it is put into a tri-state when the NCS pin is high. The CLK pin clocks the diagnostic shift register. New SDO data will appear on every rising edge of this pin and new SDI data will be latched on every CLK's falling edge into the shift register. With the first positive pulse of the CLK, the failure register will be cleared. There is no bus collision at a small spike at the NCS. The CLK is always LOW while the NCS-signal is changing.

RESET

There are two different reset functions realized :

Under voltage reset : as long as the V_{CC} voltage is lower than V_{CCRES}, the power stages are switched off and the failure-registers are reset.

Reset pin : as long as the NRES-pin is low, following circuits are reset :

- Power stages
- Failure register

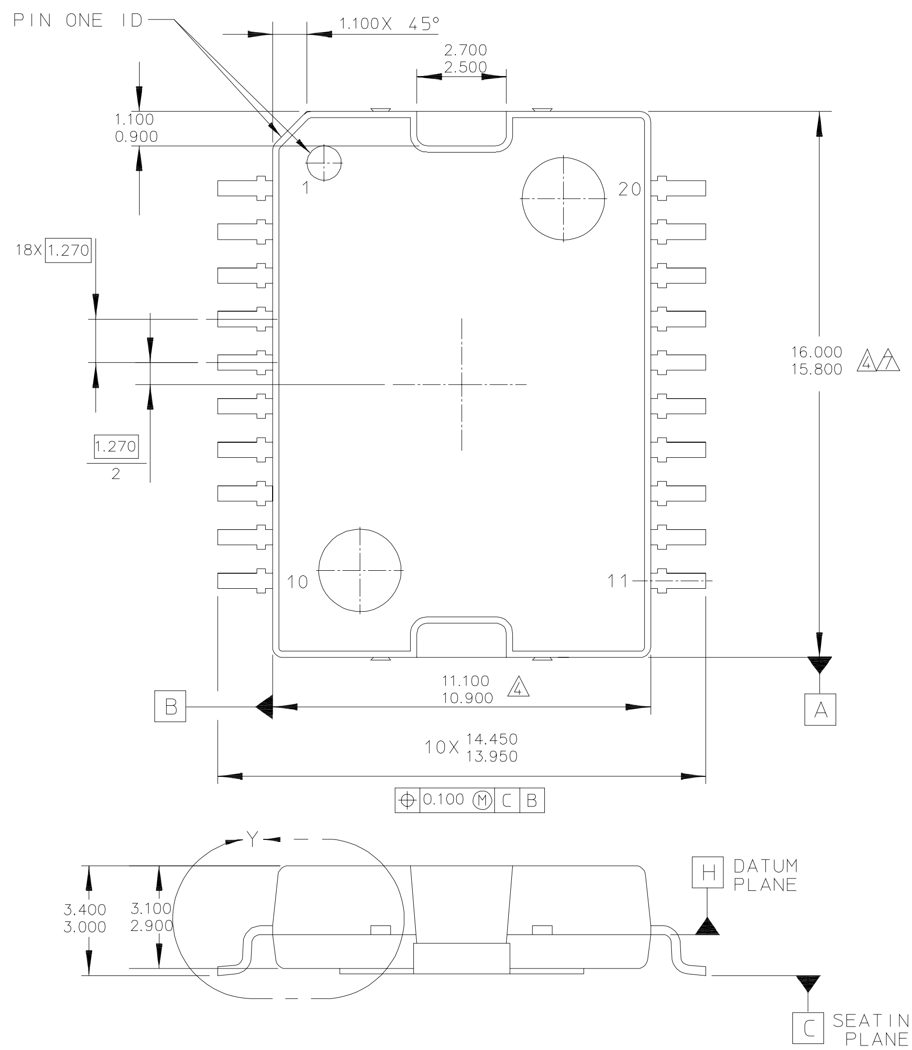
UNDERVOLTAGE PROTECTION

At low V_{CC} voltage, the device remains switched off even if there is a voltage ramp at the OUT pin.

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.



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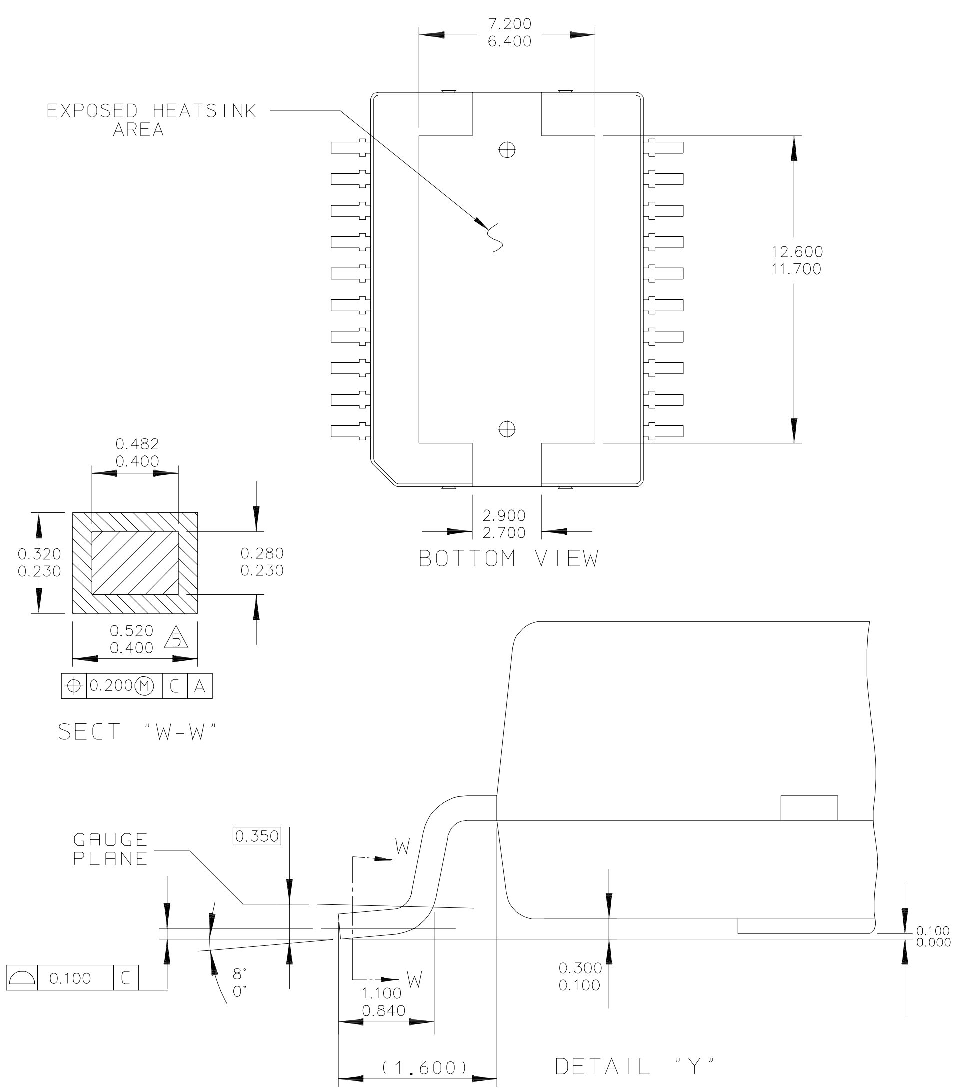
	CASE NUMBER: 979	11 OCT 2005
	STANDARD: NON-JEDEC	

DH SUFFIX
VW (PB-FREE) SUFFIX
20-PIN HSOP
PLASTIC PACKAGE
98ASH70702A
ISSUE B

PACKAGE DIMENSIONS (CONTINUED)



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	CASE NUMBER: 979	11 OCT 2005
	STANDARD: NON-JEDEC	

DH SUFFIX
VW (PB-FREE) SUFFIX
20-PIN HSOP
PLASTIC PACKAGE
98ASH70702A
ISSUE B

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
6.0	11/2006	• Implemented Revision History page • Added Pb-Free suffix code VW • Converted to Freescale format, and adjusted to the prevailing form and style

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