MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

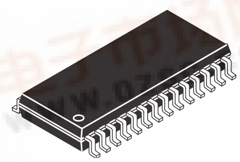
Document order number: MC33742
Rev 2.0, 10/2004

Advance Information

33742
33742S

System Basis Chip (SBC) with Enhanced High-Speed CAN Transceiver

SYSTEM BASIS CHIP WITH ENHANCED HIGH-SPEED CAN



DW SUFFIX
CASE 751F-05
28-TERMINAL SOICW

The 33742 and the 33742S are monolithic integrated circuits combining many functions frequently used by automotive environmental control units (ECUs).

The 33742 is an SBC having a fully protected fixed 5.0 V low-drop regulator with current limit, overtemperature pre-warning, and reset. An output drive with sense input is also provided to implement a second 5.0 V regulator, using an external PNP bipolar junction transistor. The 33742 has normal, standby, stop, and sleep modes, an internally switched high-side power supply output with four wake-up inputs, programmable window watchdog, interrupt, reset, SPI input control, and a high-speed CAN transceiver compatible with CAN 2.0 A and B protocols for module-to-module communication.

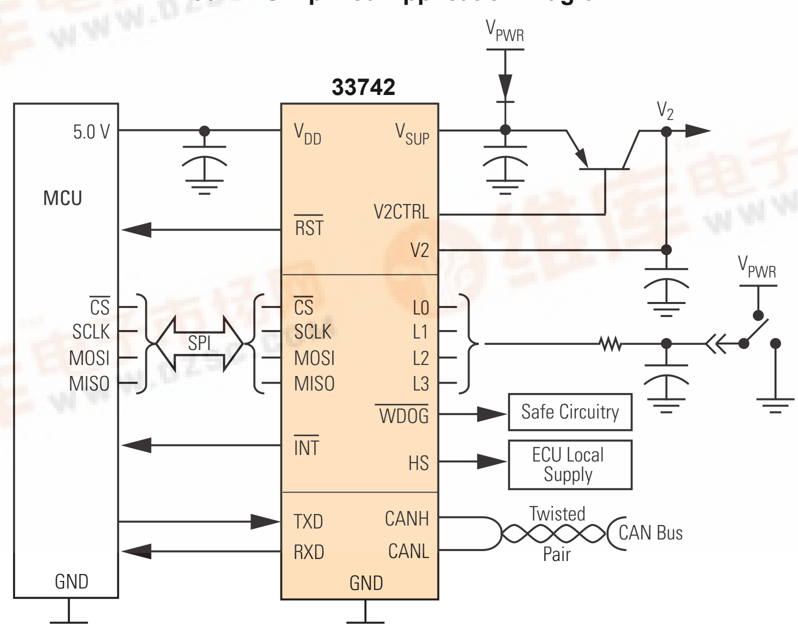
Features

- High-Speed 1.0 Mbps CAN Interface with Bus Diagnostic Capability (Detection of CANH and CANL Short to Ground, to V_{DD}, and to V_{SUP})
- Low-Drop Voltage 5.0 V, 200 mA V_{DD} Regulator with Current-Limiting, Overtemperature Pre-Warning, and Output Monitoring with Reset
- Additional 5.0 V Regulator with External Series Pass Transistor
- Normal, Standby, Stop, and Sleep Modes with Low Sleep and Stop Mode Current
- 150 mA High-Side Switch Output for Control of External Circuitry
- Four External Wake-Up Inputs
- Software-Programmable Watchdog Window, Interrupt, and Reset

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33742DW/R2	-40°C to 125°C	28 SOICW
MC33742SDW/R2	-40°C to 125°C	28 SOICW

33742 Simplified Application Diagram



This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table 1. Significance Device Differences

Motorola Part No.	Reset Duration	Device Differences	See Page
33742	15 ms (typical)	The duration of the reset mode, in which the $\overline{RST}$ terminal is asserted low, is 15 ms typical. Reset mode is entered after device power up, when a V_{DD} undervoltage condition occurred and if the watchdog register is not properly triggered.	15
33742S	3.5 ms (typical)	The duration of the reset mode, in which the $\overline{RST}$ terminal is asserted low, is 3.5 ms typical. Reset mode is entered after device power up, when a V_{DD} undervoltage condition occurred and if the watchdog register is not properly triggered.	15

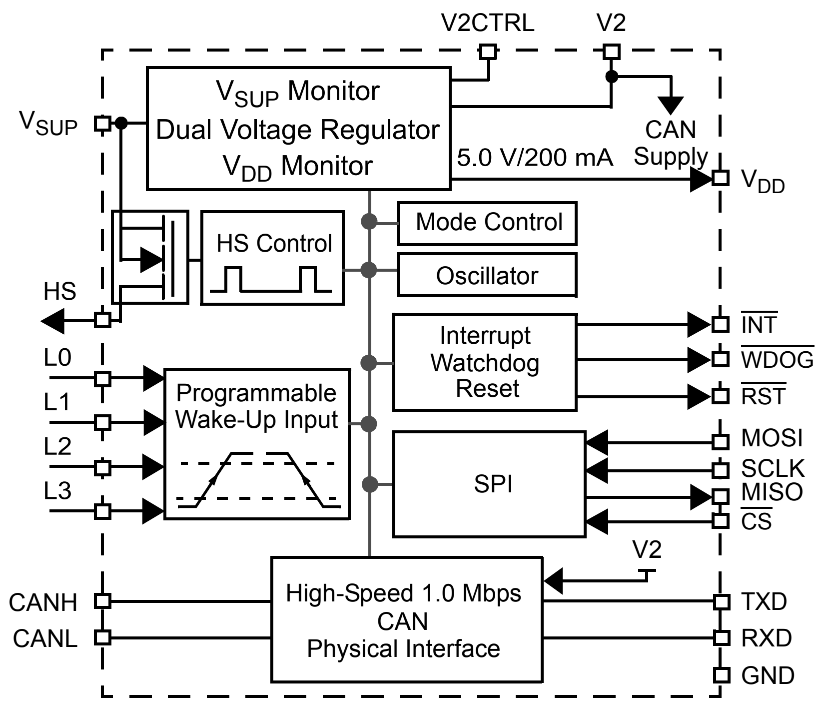
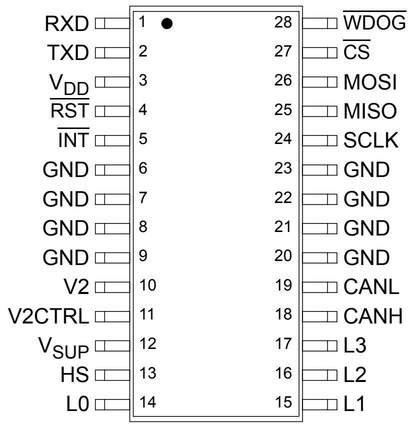


Figure 1. 33742 Simplified Internal Block Diagram



TERMINAL DEFINITIONS

A functional description of each terminal can be found in the System/Application Information section beginning on page 18.

Terminal	Terminal Name	Formal Name	Definition
1	RXD	Receive Data	CAN bus receive data output
2	TXD	Transmit Data	CAN bus transmit data input
3	V_{DD}	Voltage Digital Drain	5.0 V regulator output terminal.
4	$\overline{RST}$	Reset Output (Active LOW)	This is the device reset output whose main function is to reset the MCU. This terminal has an internal pull-up current source to V_{DD}
5	$\overline{INT}$	Interrupt Output (Active LOW)	This output is asserted LOW when an enabled interrupt condition occurs. The output is a push-pull structure.
6–9 20–23	GND	Ground	Ground of the IC. These terminals are connected to the package lead frame in order to provide a thermal path.
10	V2	Voltage Source 2	Sense input for V2 regulator using external ballast. V2 is also the internal supply for the CAN cell.
11	V2CTRL	Voltage Source 2 Control	Output driver for the external ballast transistor.
12	V_{SUP}	Voltage Supply	Supply input for the complete device.
13	HS	High-Side Output	Output of internal high-side switch. Current capability is internally limited to 150 mA.
14–17	L0–L3	Level 0–3 Inputs	Input interfaces to external circuitry (switched or ICs). Levels at these terminals can be read by SPI and input can be used as programmable wake-up input in Sleep or Stop mode.
18	CANH	CAN High	CAN high output.
19	CANL	CAN Low	CAN low output.
24	SCLK	Serial Data Clock	Clock input for the Serial Peripheral Interface (SPI) of the device.
25	MISO	Master In/Slave Out	SPI data sent to MCU. When $\overline{CS}$ is HIGH, terminal is high impedance.
26	MOSI	Master Out/Slave In	SPI data received by the 33742.
27	$\overline{CS}$	Chip Select (Active LOW)	Chip select terminal for SPI. When $\overline{CS}$ is LOW, device is selected.
28	$\overline{WDOG}$	Watchdog Output (Active LOW)	Output of watchdog circuitry. Terminal is asserted LOW if software watchdog is not correctly triggered.

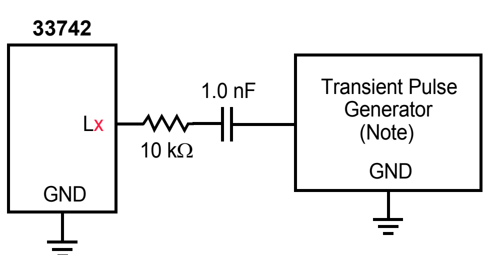
MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
ELECTRICAL RATINGS			
Power Supply Voltage at V_{SUP} Terminal Continuous (Steady-State) Transient Voltage (Load Dump)	V_{SUP}	 -0.3 to 27 -0.3 to 40	V
Logic Inputs (RXD, TXD, MOSI, MISO, $\overline{CS}$, SCLK, $\overline{RST}$, $\overline{WDOG}$, and $\overline{INT}$ Terminals)	V_{LOG}	-0.3 to V_{DD} + 0.3	V
Output Current at V_{DD} Terminal	I_{DD}	Internally Limited	A
HS Terminal Voltage Output Current	 V_{HS} I_{HS}	 -0.3 to V_{SUP} + 0.3 Internally Limited	 V A
ESD Voltage, Human Body Model (Note 1) HS, L0, L1, L2, L3, CANH, CANL Terminals All Other Terminals	V_{ESD1}	 ±4000 ±2000	V
ESD Voltage, Machine Model (Note 2)	V_{ESD2}	±200	V
L0, L1, L2, L3 Terminals DC Input Voltage DC Input Current Transient Input Voltage with External Component (Note 3)	 V_{DCIN} I_{DCIN} V_{TRINEC}	 -0.3 to 40 ±2.0 ±100	 V mA V
Power Dissipation (Note 4)	P_D	1.0	W
CANL and CANH Terminals Continuous Voltage Continuous Current	 $V_{CANH/L}$ $I_{CANH/L}$	 -27 to 40 200	 V mA
CANH and CANL Transient Voltage (Load Dump) (Note 5)	$V_{LDH/L}$	40	V
CANH and CANL Transient Voltage (Note 6)	$V_{TRH/L}$	±40	V

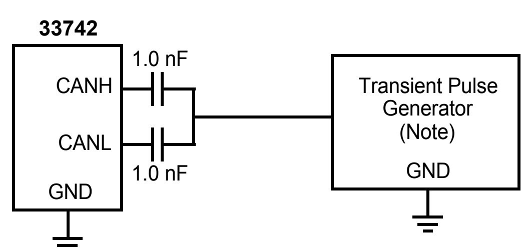
Notes

1. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
2. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
3. Testing in accordance with ISO 7637-1. See also Figure 2.
4. Maximum power dissipation at 85°C ambient temperature in free air with no heatsink, according to JEDEC JESD51-2 and JESD51-3 specifications.
5. Load dump test in accordance with ISO 7637-1.
6. Transient test in accordance with ISO 7637-1. See also Figure 3.



Note Waveform per ISO 7637-1. Test Pulses 1, 2, 3a, and 3b.

Figure 2. ISO 7637 Test Setup for L0:L3 Inputs



Note Waveform per ISO 7637-1. Test Pulses 1, 2, 3a, and 3b.

Figure 3. ISO 7637 Test Setup for CANH/CANL

MAXIMUM RATINGS (continued)

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
THERMAL RATINGS			
Operating Temperature Ambient Junction	 T_A T_J	 -40 to 125 -40 to 150	°C
Storage Temperature	T_{STG}	-55 to 165	°C
Thermal Resistance Junction to GND Terminals	$R_{\theta JG}$	20	°C/W
Peak Package Reflow Temperature During Solder Mounting (Note 7)	T_{SOLDER}	240	°C

Notes

7. Terminal soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40°C ≤ T_A ≤ 125°C. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
V_{SUP} TERMINAL					
Nominal DC Supply Voltage	V_{SUP}	5.5	–	18	V
Extended DC Voltage	V_{SUP-EX}				V
Full Functionality (Note 8)		18	–	27	
Reduced Functionality (Note 9)		4.5	–	5.5	
Input Voltage During Load Dump	V_{SUP-LD}	–	–	40	V
Input Voltage During Jump Start	V_{SUP-JS}	–	–	27	V
Supply Current in Standby Mode (Note 10) (I_{OUT} at V_{DD} = 10 mA, CAN Recessive or Sleep Mode)	$I_{SUP(STDBY)}$				mA
T_A ≥ 25°C		–	12	15	
T_A = -40°C to 25°C		–	14.5	19	
Supply Current in Normal Mode (Note 10) (I_{OUT} at V_{DD} = 10 mA, CAN Recessive or Sleep Mode)	$I_{SUP(NORM)}$				mA
T_A ≥ 25°C		–	12.4	15	
T_A = -40°C to 25°C		–	15	19	
Supply Current in Sleep Mode (Note 10) [V_{DD} and V2 OFF, CAN in Sleep Mode with CAN Wake-Up Disabled (Note 11)]	$I_{SUP(SLP-WD)}$				µA
V_{SUP} < 13.5 V, Oscillator Running (Note 12)		–	85	105	
V_{SUP} < 13.5 V, Oscillator Not Running (Note 13)		–	53	80	
V_{SUP} = 18 V, Oscillator Running (Note 12)		–	110	140	
Supply Current in Sleep Mode (Note 10) [V_{DD} and V2 OFF, V_{SUP} < 13.5 V, Oscillator Not Running (Note 13), CAN in Sleep Mode with Wake-Up Enabled]	$I_{SUP(SLP-WE)}$				µA
T_A = -40°C		–	80	–	
T_A = 25°C		–	65	–	
T_A = 125°C		–	55	–	
Supply Current in Stop Mode (Note 10) [I_{OUT} at V_{DD} < 2.0 mA, V_{DD} ON, CAN in Sleep Mode with Wake-Up Disabled (Note 11)	$I_{SUP(STOP-WD)}$				µA
V_{SUP} < 13.5 V, Oscillator Running (Note 12)		–	–	160	
V_{SUP} < 13.5 V, Oscillator Not Running (Note 13)		–	80	160	
V_{SUP} = 18 V, Oscillator Running (Note 12)		–	100	210	

Notes

8. All functions and modes available and operating. Watchdog, HS turn ON/turn OFF, CAN cell operating, L0:L3 inputs operating, SPI read/write operation. Overtemperature may occur.
9. V_{DD} > 4.0 V, $\overline{RST}$ HIGH if reset 2 selected by SPI, logic terminal high level reduced, device is functional.
10. Current measured at V_{SUP} terminal.
11. If CAN cell is Sleep-Enabled for wake-up, an additional current ($I_{CAN-SLEEP}$) must be added to specified value.
12. Oscillator running means one of the following function is active: Forced Wake-Up *or* Cyclic Sense *or* Software Watchdog in Stop mode.
13. Oscillator not running means none of the following functions are active: Forced Wake-Up *and* Cyclic Sense *and* Software Watchdog in Stop mode.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40°C ≤ T_A ≤ 125°C. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
V_{SUP} TERMINAL (continued)					
Supply Current in Stop Mode (Note 14) [I_{OUT} at V_{DD} < 2.0 mA, V_{DD} ON, V_{SUP} < 13.5 V, Oscillator Not Running (Note 15), CAN in Sleep Mode with Wake-Up Enabled]	$I_{SUP(STOP-WE)}$				µA
T_A = -40°C		–	100	–	
T_A = 25°C		–	92	–	
T_A = 125°C		–	80	–	
BATFAIL Flag Internal Threshold	V_{BF}	1.5	3.0	4.0	V
BATFAIL Flag Hysteresis (Note 16)	$V_{BF(HYS)}$	–	1.0	–	V
Battery Fall Early Warning Threshold	$V_{BF(EW)}$				V
In Normal and Standby Modes		5.3	5.8	6.3	
Battery Fall Early Warning Hysteresis	$V_{BF(EW-HYST)}$				V
In Normal and Standby Modes (Note 16)		0.1	0.2	0.3	
V_{DD} TERMINAL (Note 17)					
V_{DD} Output Voltage (2.0 mA < I_{DD} < 200 mA)	V_{DDOUT}				V
5.5 V < V_{SUP} < 27 V		4.9	5.0	5.1	
4.5 V < V_{SUP} < 5.5 V		4.0	–	–	
Dropout Voltage	V_{DDDRP1}				V
I_{DD} = 200 mA		–	0.2	0.5	
Dropout Voltage, Limited Output Current and Low V_{SUP}	V_{DDDRP2}				V
I_{DD} = 50 mA, 4.5 V < V_{SUP}		–	0.1	0.25	
V_{DD} Output Current	I_{DD}				mA
Internally Limited		200	285	350	
Thermal Shutdown (Junction)	T_{SD}				°C
Normal or Standby Mode		160	–	200	
Overtemperature Pre-Warning (Junction)	T_{PW}				°C
VDDTEMP Bit Set		125	–	160	
Temperature Threshold Difference	$T_{SD} - T_{PW}$	20	–	40	°C
$\overline{RST}$ Threshold, Selectable by RSTTH Bit in SPI Register RCR	$V_{\overline{RST}TH}$				V
Threshold 1, Default Value after Reset, RSTTH Bit set to 0		4.5	4.6	4.7	
Threshold 2, RSTTH bit Set to 1		4.0	4.2	4.3	
V_{DD} for Reset Active	V_{DDR}	1.0	–	$V_{\overline{RST}TH}$	V

Notes

14. Current measured at V_{SUP} terminal.
15. Oscillator not running means none of the following functions are active: Forced Wake-Up *and* Cyclic Sense *and* Software Watchdog in Stop mode.
16. Guaranteed by design; however, it is not production tested.
17. I_{DD} is the total regulator output current. V_{DD} specification with external capacitor. Stability requirement: Capacitance > 47 µF, ESR < 1.3 Ω (tantalum capacitor). In Reset, Normal Request, Normal and Standby modes. Measures with capacitance = 47 µF tantalum.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40°C ≤ T_A ≤ 125°C. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
V_{DD} TERMINAL (continued) (Note 18)					
Line Regulation (I_{DD} = 10 mA, Capacitance = 47 µF Tantalum at V_{DD}) 9.0 V < V_{SUP} < 18 V 5.5 V < V_{SUP} < 27 V	V_{LR}	 – –	 5.0 10	 25 25	mV
Load Regulation (Capacitance = 47 µF Tantalum at V_{DD}) 1.0 mA < I_{DD} < 200 mA	V_{LD}	 –	 25	 75	mV
Thermal Stability V_{SUP} = 13.5 V, I_{DD} = 100 mA (Note 19)	$V_{THERM-S}$	 –	 30	 50	mV
V_{DD} TERMINAL IN STOP MODE (Note 18)					
V_{DD} Output Voltage I_{DD} ≤ 2.0 mA I_{DD} ≤ 10 mA	V_{DDSTOP}	 4.75 4.75	 5.0 5.0	 5.25 5.25	V
I_{DD} Output Current to Wake-Up	I_{DDS-WU}	10	17	25	mA
Reset Threshold Selectable by SPI, Default Value after Reset, Bit Value 0 Selectable by SPI, Bit Value 1	$V_{\overline{RST}-STOP}$	 4.5 4.1	 4.6 4.2	 4.7 4.3	V
Line Regulation (Capacitance = 47 µF Tantalum at V_{DD}) 5.5 V < V_{SUP} < 27 V, I_{DD} = 2.0 mA	$V_{LR-STOP}$	 –	 5.0	 25	mV
Load Regulation (Capacitance = 47 µF Tantalum at V_{DD}) 1.0 mA < I_{DD} < 10 mA	$V_{LD-STOP}$	 –	 15	 75	mV
V2 TRACKING VOLTAGE REGULATOR (Note 20)					
V2 Output Voltage (Capacitance = 10 µF Tantalum at V2) 2.0 mA ≤ I_2 ≤ 200 mA, 5.5 V < V_{SUP} < 27 V	V_2	 0.99	 1.0	 1.01	V_{DD}
I_2 Output Current (for Information Only) Depending on External Ballast Transistor	I_2	 200	 –	 –	mA
V2 Control Drive Current Capability (Note 21) Worst Case at T_J = 125°C	I_{2CTRL}	 0	 –	 10	mA
V2LOW Flag Threshold	V_{2LTH}	3.75	4.0	4.25	V

Notes

18. I_{DD} is the total regulator output current. V_{DD} specification with external capacitor. Stability requirement: capacitance > 47 µF, ESR < 1.3 Ω (tantalum capacitor). In Reset, Normal Request, Normal and Standby modes, measures with capacitance = 47 µF tantalum.
19. Guaranteed by characterization and design; however, it is not production tested.
20. V2 specification with external capacitor. Stability requirement: capacitance > 42 µF and ESR < 1.3 Ω (tantalum capacitor), external resistor between base and emitter required. Measurement conditions: ballast transistor MJD32C, capacitance > 10 µF tantalum, 2.2 kΩ resistor between base and emitter of ballast transistor.
21. Guaranteed current capability of the V2CTRL terminal is 10 mA. Current may be higher. No active limitation is provided.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40°C ≤ T_A ≤ 125°C. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC OUTPUT TERMINAL (MISO) (Note 22)					
Low-Level Output Voltage I_{OUT} = 1.5 mA	V_{OL}	0	–	1.0	V
High-Level Output Voltage I_{OUT} = -250 µA	V_{OH}	V_{DD}-0.9	–	V_{DD}	V
Tri-Stated MISO Leakage Current 0 V < V_{MISO} < V_{DD}	I_{HZ}	-2.0	–	2.0	µA
LOGIC INPUT TERMINALS (MOSI, SCLK, $\overline{CS}$)					
High-Level Input Voltage	V_{IH}	0.7 V_{DD}	–	V_{DD} + 0.3	V
Low-Level Input Voltage	V_{IL}	-0.3	–	0.3 V_{DD}	V
High-Level Input Current on $\overline{CS}$ V_I = 4.0 V	I_{IH}	-100	–	-20	µA
Low-Level Input Current on $\overline{CS}$ V_I = 1.0 V	I_{IL}	-100	–	-20	µA
MOSI and SCLK Input Current 0 V < V_{IN} < V_{DD}	I_{IN}	-10	–	10	µA
$\overline{RST}$ OUTPUT TERMINAL (Note 23)					
High-Level Output Current 0 V < V_{OUT} < 0.7 V_{DD}	I_{OH}	-300	-250	-150	µA
Low-Level Output Voltage I_O = 1.5 mA, 5.5 V < V_{SUP} < 27 V I_O = 0 mA, 1.0 V <V_{SUP} < 5.5 V	V_{OL}	 0 0	 – –	 0.9 0.9	V
$\overline{RST}$ Pulldown Current V > 0.9 V	I_{PDW}	2.3	–	5.0	mA
$\overline{WDOG}$ OUTPUT TERMINAL (Note 24)					
Low-Level Output Voltage I_O = 1.5 mA, 1.0 V < V_{SUP} < 27 V	V_{OL}	0	–	0.9	V
High-Level Output Voltage I_O = -250 µA	V_{OH}	V_{DD}-0.9	–	V_{DD}	V
$\overline{INT}$ OUTPUT TERMINAL (Note 24)					
Low-Level Output Voltage I_O = 1.5 mA	V_{OL}	0	–	0.9	V
High-Level Output Voltage I_O = -250 µA	V_{OH}	V_{DD}-0.9	–	V_{DD}	V

Notes

22. Push-pull structure with tri-state condition ($\overline{CS}$ HIGH).
23. Output terminal only. Supply from V_{DD}. Structure switch to ground with pullup current source.
24. Push-pull structure.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40°C ≤ T_A ≤ 125°C. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HS OUTPUT TERMINAL					
Driver Output ON Resistance	$R_{DS(ON)}$				Ω
T_J = 25°C, I_{OUT} - 150 mA, V_{SUP} > 9.0 V		–	2.0	2.5	
T_A = 125°C, I_{OUT} - 150 mA, V_{SUP} > 9.0 V		–	–	4.5	
T_A = 125°C, I_{OUT} - 120 mA, 5.5 V < V_{SUP} < 9.0 V		–	3.5	5.5	
Output Current Limitation	I_{LIM}				mA
V_{SUP} - V_{HS} > 1.0 V		160	–	500	
HS Thermal Shutdown	T_{SD}	155	–	190	°C
HS Leakage Current	I_{LEAK}	–	–	10	µA
Output Clamp Voltage	V_{CL}				V
I_{OUT} = -10 mA, No Inductive Load Drive Capability		-1.5	–	-0.3	
L0, L2, L2, AND L3 INPUT TERMINALS					
Negative Switching Threshold	V_{THN}				V
5.5 V < V_{SUP} < 6.0 V		2.0	2.5	3.0	
6.0 V < V_{SUP} < 18 V		2.5	3.0	3.6	
18 V < V_{SUP} < 27 V		2.7	3.2	3.7	
Positive Switching Threshold	V_{THP}				V
5.5 V < V_{SUP} < 6.0 V		2.7	3.3	3.8	
6.0 V < V_{SUP} < 18 V		3.0	4.0	4.6	
18 V < V_{SUP} < 27 V		3.5	4.2	4.7	
Hysteresis	V_{HYST}				V
5.5 V < V_{SUP} < 27 V		0.6	–	1.3	
Input Current	I_{IN}				µA
-0.2 V < V_{IN} < 40 V		-10	–	10	
CAN SUPPLY					
Supply Current of CAN Cell					
CAN in Normal Mode, Bus Recessive State	I_{RES}	–	1.3	3.0	mA
CAN in Normal Mode, Bus Dominant State without Bus Load	I_{DOM}	–	1.5	3.5	mA
CAN in Sleep State, Wake-Up Enabled, V2 Regulator OFF	$I_{CAN-SLEEP}$	–	12	24	µA
CAN in Sleep State, Wake-Up Disabled, V2 Regulator OFF (Note 25)	I_{DIS}	–	–	1.0	µA

Notes

25. Guaranteed by design; however, it is not production tested.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40°C ≤ T_A ≤ 125°C. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CANH AND CANL TERMINALS					
Bus Terminals Common Mode Voltage	V_{CM}	-27	–	40	V
Differential Input Voltage (Common Mode Between -3.0 V and 7.0 V)	V_{CANH} - V_{CANL}				mV
Recessive State at RXD		–	–	500	
Dominant State at RXD		900	–	–	
Differential Input Hysteresis (RXD)	V_{HYST}	100	–	–	mV
Input Resistance	R_{IN}	5.0	–	100	kΩ
Differential Input Resistance	R_{IND}	10	–	100	kΩ
CANH Output Voltage	V_{CANH}				V
TXD Dominant State		2.75	–	4.5	
TXD Recessive State		–	–	3.0	
CANL Output Voltage	V_{CANL}				V
TXD Dominant State		0.5	–	2.25	
TXD Recessive State		2.0	–	–	
Differential Output Voltage	Vo_H-Vo_L				
TXD Dominant State		1.5	–	3.0	V
TXD Recessive State		–	–	100	mV
Output Current Capability (Dominant State)					mA
CANH	I_{CANH}	–	–	-35	
CANL	I_{CANL}	35	–	–	
Overtemperature Shutdown	T_{SD}	160	180	–	°C
CANL Overcurrent Detection (Note 26)					mA
CANL	$I_{CANL/OC}$	60	–	200	
CANH	$I_{CANH/OC}$	-200	–	-60	
CANH and CANL Input Current, Device Supplied (CAN Sleep Mode with CAN Wake-Up Enabled or Disabled)	I_{CAN1}				µA
V_{CANH}, V_{CANL} from 0 V to 5.0 V		–	3.0	10	
V_{CANH}, V_{CANL} = -2.0 V		-60	-50	–	
V_{CANH}, V_{CANL} = 7.0 V		–	60	75	
CANH and CANL Input Current, Device Unsupplied	I_{CAN2}				µA
V_{CANH}, V_{CANL} = 2.5 V		–	40	100	
V_{CANH}, V_{CANL} = -2.0 V		-60	-50	–	
V_{CANH}, V_{CANL} = 7.0 V		–	190	240	

Notes

26. Reported in CAN register. For a description of the contents of the CAN register, refer to CAN Register (CAN) on page 40.

STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40°C ≤ T_A ≤ 125°C. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CANH AND CANL DIAGNOSTIC INFORMATION					
CANL to GND Threshold	V_{LG}	–	1.75	–	V
CANH to GND Threshold	V_{HG}	–	1.75	–	V
CANL to V_{SUP} Threshold	V_{LVB}	–	V_{SUP} - 2.0	–	V
CANH to V_{SUP} Threshold	V_{HVB}	–	V_{SUP} - 2.0	–	V
CANL to V_{DD} Threshold	V_{L5}	–	V_{DD} - 0.43	–	V
CANH to V_{DD} Threshold	V_{H5}	–	V_{DD} - 0.43	–	V
RXD Weak Pulldown Current Source (Note 27) RXD Permanent Dominant Failure Condition	I_{RXDW}	–	100	–	µA
TXD AND RXD TERMINALS					
TXD Input High Voltage	V_{IH}	0.7 V_{DD}	–	V_{DD} + 0.4	V
TXD Input Low Voltage	V_{IL}	-0.4	–	0.3 V_{DD}	V
TXD High-Level Input Current V_{TXD} = V_2	I_{IH}	-10	–	10	µA
TXD Low-Level Input Current V_{TXD} = 0 V	I_{IL}	-150	-100	-50	µA
RXD Output High Voltage I_{RXD} = 250 µA	V_{OH}	V_{DD} - 1.0	–	–	V
RXD Output Low Voltage I_{RXD} = 1.0 mA	V_{OL}	–	–	0.5	V

Notes

27. Guaranteed by design; however, it is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40°C ≤ T_A ≤ 125°C. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE TIMING (Note 28)					
SPI Operation Frequency	f_{REQ}	0.25	–	4.0	MHz
SCLK Clock Period	t_{PCLK}	250	–	N/A	ns
SCLK Clock High Time	t_{WSCLKH}	125	–	N/A	ns
SCLK Clock Low Time	t_{WSCLKL}	125	–	N/A	ns
Falling Edge of $\overline{CS}$ to Rising Edge of SCLK	t_{LEAD}	100	–	N/A	ns
Falling Edge of SCLK to Rising Edge of $\overline{CS}$	t_{LAG}	100	–	N/A	ns
MOSI to Falling Edge of SCLK	t_{SISU}	40	–	N/A	ns
Falling Edge of SCLK to MOSI	t_{SIH}	40	–	N/A	ns
MISO Rise Time (Note 29) C_L = 220 pF	t_{RSO}	–	25	50	ns
MISO Fall Time (Note 29) C_L = 220 pF	t_{FSO}	–	25	50	ns
Time from Falling or Rising Edges of $\overline{CS}$ MISO Low Impedance MISO High Impedance	 t_{SOEN} t_{SODIS}	 – –	 – –	 50 50	ns
Time from Rising Edge of SCLK to MISO Data Valid 0.2 V_{DD} ≤ MISO ≥ 0.8 V_{DD}, C_L = 200 pF	t_{VALID}	–	–	50	ns
STATE MACHINE TIMING					
Delay Between $\overline{CS}$ LOW-to-HIGH Transition (at End of SPI Stop Command) and Stop Mode Activation (Note 30)	$t_{\overline{CS}\text{-}STOP}$	18	–	34	µs
Interrupt Low-Level Duration Stop Mode	$t_{\overline{INT}}$	7.0	10	13	µs
Internal Oscillator Frequency (Note 31)	f_{OSC}	–	100	–	kHz
Watchdog Period Normal and Standby Modes Period 1 Period 2 Period 3 Period 4	t_{WD}	 8.58 39.6 88 308	 9.75 45 100 350	 10.92 50.4 112 392	ms

Notes

28. See Figure 4, SPI Timing Diagram, page 17.
29. Not production tested. Guaranteed by design.
30. Not production tested. Guaranteed by design. Detected by V2 OFF.
31. f_{OSC} is indirectly measured (1.0 ms reset) and trimmed.

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40°C ≤ T_A ≤ 125°C. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
STATE MACHINE TIMING (continued)					
Normal Request Mode Timeout Normal Request Mode	t_{NRTOUT}	308	350	392	ms
Watchdog Period Stop Mode Period 1 Period 2 Period 3 Period 4	$t_{WD\text{-}STOP}$	 6.82 31.5 70 245	 9.75 45 100 350	 12.7 58.5 130 455	ms
Watchdog Period Accuracy Normal and Standby Modes Stop Mode	f_{ACC}	 -12 -30	 – –	 12 30	%
Cyclic Sense/FWU Timing Sleep and Stop Modes Timing 1 Timing 2 Timing 3 Timing 4 Timing 5 Timing 6 Timing 7 Timing 8	t_{CSFWU}	 3.22 6.47 12.9 25.9 51.8 66.8 134 271	 4.6 9.25 18.5 37 74 95.5 191 388	 5.98 12 24 48.1 96.2 124 248 504	ms
Cyclic Sense ON Time Sleep and Stop Modes.	t_{ON}	200	350	500	µs
Cyclic Sense/FWU Timing Accuracy Sleep and Stop Modes	t_{ACC}	-30	–	30	%
Delay Between SPI Command and HS Turn ON (Note 32) Normal or Standby Mode, V_{SUP} > 9.0 V	$t_{S\text{-}HSON}$	–	–	22	µs
Delay Between SPI Command and HS Turn OFF (Note 32) Normal or Standby Mode, V_{SUP} > 9.0 V	$t_{S\text{-}HSOFF}$	–	–	22	µs
Delay Between SPI and V2 Turn ON (Note 32) Standby Mode	$t_{S\text{-}V2ON}$	9.0	–	22	µs
Delay Between SPI and V2 Turn OFF (Note 32) Normal Mode	$t_{S\text{-}V2OFF}$	9.0	–	22	µs
Delay Between Normal Request and Normal Mode After Watchdog Trigger Command (Note 32) Normal Request Mode	$t_{S\text{-}NR2N}$	15	35	70	µs
Delay Between SPI and CAN Normal Mode (Note 32) Normal Mode (Note 33)	$t_{S\text{-}CAN\_N}$	–	–	10	µs
Delay Between SPI and CAN Sleep Mode (Note 32) Normal Mode (Note 33)	$t_{S\text{-}CAN\_S}$	–	–	10	µs

Notes

32. Delay starts at falling edge of clock cycle #8 of the SPI command and start of “Turn ON” or “Turn OFF” of HS or V2.
33. Guaranteed by design; however, it is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40°C ≤ T_A ≤ 125°C. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
STATE MACHINE TIMING (continued)					
Delay Between $\overline{CS}$ Wake-Up ($\overline{CS}$ LOW to HIGH) and Device in Normal Request Mode (V_{DD} ON and $\overline{RST}$ HIGH)	$t_{W-\overline{CS}}$				µs
Stop Mode		15	40	90	
Delay Between $\overline{CS}$ Wake-Up ($\overline{CS}$ LOW to HIGH) and First Accepted SPI Command	t_{W-SPI}				µs
Device in Stop Mode After Wake-Up		90	–	N/A	
Delay Between $\overline{INT}$ Pulse and First SPI Command Accepted	$t_{S-1STSPI}$				µs
Device in Stop Mode After Wake-Up		20	–	N/A	
Delay Between Two SPI Messages Addressing the Same Register	t_{2SPI}	25	–	–	µs
V_{DD} TERMINAL					
Reset Delay Time	t_D				µs
Measured at 50% of Reset Signal		4.0	–	30	
I_{DD} Overcurrent to Wake-Up Deglitcher Time (Note 34)	$t_{IDD-DGLT}$	40	55	75	µs
$\overline{RST}$ TERMINAL					
Reset Duration After V_{DD} HIGH					ms
33742	$t_{\overline{RST}DUR}$	12	15	18	
33742S	$t_{\overline{RST}DURS}$	3.0	3.5	4.0	
L0, L2, L2, AND L3 INPUT TERMINALS					
Wake-Up Filter Time	t_{WUF}	8.0	20	38	µs

Notes

34. Guaranteed by design; however, it is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

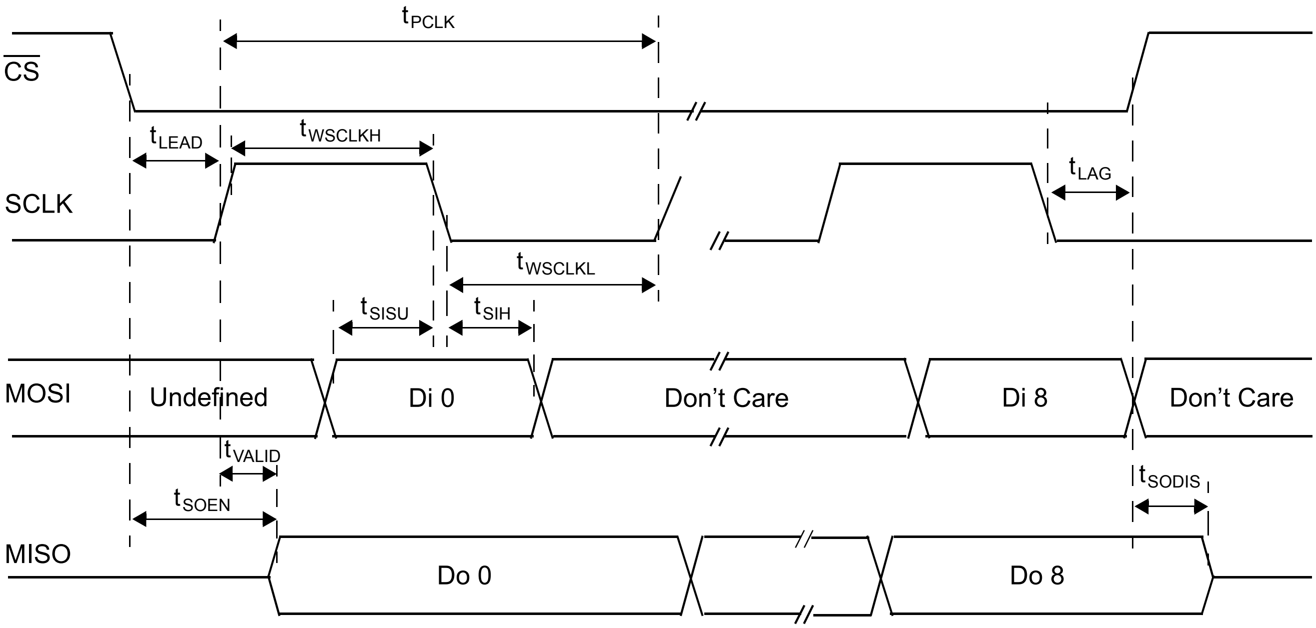
Characteristics noted under conditions 4.75 V ≤ V2 ≤ 5.25 V, 5.5 V ≤ V_{SUP} ≤ 18 V, and -40°C ≤ T_A ≤ 125°C. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CAN MODULE TIMING					
Dominant State Timeout	t_{DOUT}	200	360	520	µs
Propagation Loop Delay TXD to RXD (Recessive to Dominant) (Note 35)	t_{LRD}				ns
Slew Rate 3		60	100	210	
Slew Rate 2		70	110	225	
Slew Rate 1		80	130	255	
Slew Rate 0		110	200	310	
Propagation Delay TXD to CAN (Recessive to Dominant) (Note 36)	t_{TRD}				ns
Slew Rate 3		20	65	110	
Slew Rate 2		25	80	150	
Slew Rate 1		35	100	200	
Slew Rate 0		50	160	300	
Propagation Delay CAN to RXD (Recessive to Dominant) (Note 37)	t_{RRD}	10	50	140	ns
Propagation Loop Delay TXD to RXD (Dominant to Recessive) (Note 35)	t_{LDR}				ns
Slew Rate 3		100	150	200	
Slew Rate 2		120	165	220	
Slew Rate 1		140	200	250	
Slew Rate 0		250	340	410	
Propagation Delay TXD to CAN (Dominant to Recessive) (Note 36)	t_{TDR}				ns
Slew Rate 3		60	125	150	
Slew Rate 2		65	150	190	
Slew Rate 1		75	180	250	
Slew Rate 0		200	310	460	
Propagation Delay CAN to RXD (Dominant to Recessive) (Note 37)	t_{RDR}	20	30	60	ns
Non-Differential Slew Rate (CANL or CANH)					V/µs
Slew Rate 3	t_{SL3}	4.0	19	40	
Slew Rate 2	t_{SL2}	3.0	13.5	20	
Slew Rate 1	t_{SL1}	2.0	8.0	15	
Slew Rate 0	t_{SL0}	1.0	5.0	10	

Notes

35. See Figure 5, page 17.
36. See Figure 6, page 17.
37. See Figure 7, page 17.

Timing Diagrams



Note Incoming data at MOSI terminal is sampled by the 33742 at SCLK falling edge. Outgoing data at MISO terminal is set by the 33742 at SCLK rising edge (after t_{VALID} delay time).

Figure 4. SPI Timing Diagram

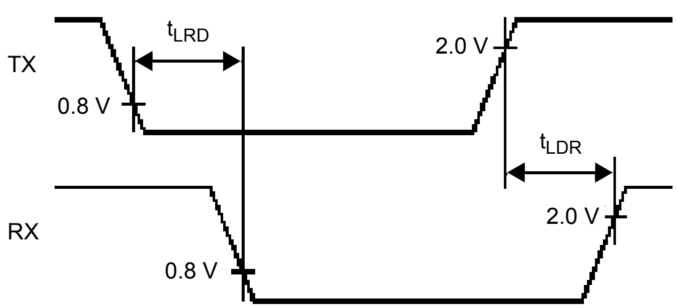


Figure 5. Propagation Loop Delay TXD to RXD

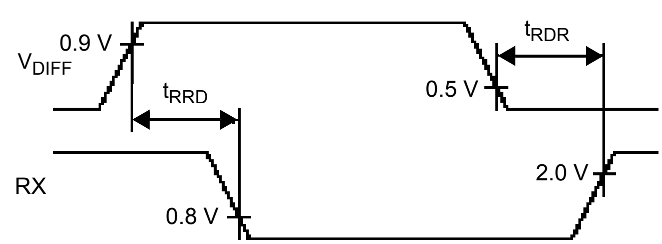


Figure 7. Propagation Delay CAN to RXD

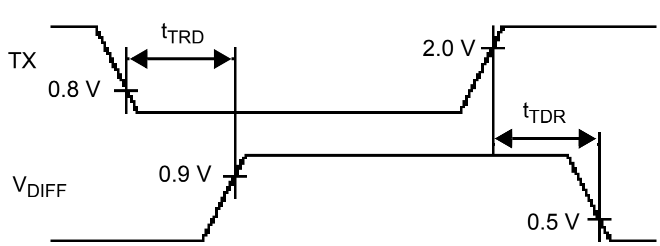


Figure 6. Propagation Delay TXD to CAN

SYSTEM/APPLICATION INFORMATION

INTRODUCTION

The 33742 and the 33742S are integrated circuits dedicated to automotive applications. Their functions include the following:

- One fully protected voltage regulator with 200 mA total output current capability available at the V_{DD} terminal.
- Driver for external pass transistor for V2 regulator function.
- V_{DD} regulator undervoltage reset function, programmable window or timeout software watchdog function.
- Two running modes: Normal and Standby modes when the microcontroller is running.
- Sleep and Stop modes for operation in low power mode to reduce the application current consumption, while offering wake-up capability from CAN interface, L3:L0 wake-up input, and automatic timer wake-up.
- Programmable wake-up input and cyclic sense wake-up.
- CAN high-speed physical interface with bus failure diagnostic and enhanced protection feature for TXD and RXD failure.
- Interface with micro through SPI. Interrupt output to report device status, diagnostic, and wake-up event.

FUNCTIONAL TERMINAL DESCRIPTION

RXD and TXD

The RXD and TXD terminals (receive data terminal and transmit data terminal, respectively) are connected to the microcontroller CAN protocol handler. TXD is an input and controls the CANH and CANL line state (dominant when TXD is LOW, recessive when TXD is HIGH). RXD is an output and reports the bus state (RXD LOW when CAN bus is dominant, HIGH when CAN bus is recessive).

V_{DD}

The V_{DD} terminal is the output terminal of the 5.0 V internal regulator. It can deliver up to 200 mA. This output is protected against overcurrent and overtemperature. It includes an overtemperature pre-warning flag, which is set when the internal regulator temperature exceeds 130°C typical. When the temperature exceeds the overtemperature shutdown (170°C typical), the regulator is turned off.

V_{DD} includes an undervoltage reset circuitry, which sets the $\overline{RST}$ terminal LOW when V_{DD} is below the undervoltage reset threshold.

$\overline{RST}$

The Reset terminal $\overline{RST}$ is an output that is set LOW when the device is in reset mode. The $\overline{RST}$ terminal is set HIGH when the device is not in reset mode. $\overline{RST}$ includes an internal pullup current source. When $\overline{RST}$ is LOW, the sink current capability is limited, allowing $\overline{RST}$ to be shorted to 5.0 V for software debug or software download purposes.

$\overline{INT}$

The Interrupt terminal $\overline{INT}$ is an output that is set LOW when an interrupt occurs. $\overline{INT}$ is enabled using the Interrupt Register (INTR). When $\overline{INT}$ occurs, $\overline{INT}$ stays LOW until the $\overline{INT}$ source is cleared.

$\overline{INT}$ output also reports a wake-up event by a 10 µs typical pulse when the device is in stop mode.

V2

The V2 terminal is the input sense of the V2 regulator. It is connected to the external ballast transistor. V2 is also the 5.0 V supply of the internal CAN interface. It is possible to connect V2 to an external 5.0 V regulator or to the V_{DD} output when no external ballast transistor is used. In this case, the V2CTRL terminal must be left open. Refer to Figure 28, 33742 Typical Application Schematic, page 46.

V2CTRL

The V2CTRL terminal is the output drive of the V2 regulator connected to the external ballast transistor.

V_{SUP}

The V_{SUP} terminal is the battery supply input of the device.

HS

The HS terminal is the internal high-side driver output. It is internally protected against overcurrent and overtemperature.

L0, L1, L2, and L3

The L0:L3 input terminals can be connected to external switches or any IC's output. The state of the inputs can be read by SPI. Theses inputs can be used as wake-up events when the device is set in Sleep or Stop mode.

CANH and CANL

The CAN High and CAN Low terminals are the interfaces to the CAN bus lines. They are controlled by TXD input level, and the state of CANH and CANL is reported through RXD output. A 60 Ω impedance termination is connected between CANH and CANL.

SCLK

This is the Serial Data Clock terminal of the serial peripheral interface.

MISO

This is the Master In/Slave Out terminal of the serial peripheral interface. Data are send from the device to the microcontroller through MISO terminal.

MOSI

This is the Master Out/Slave In terminal of the serial peripheral interface. Control data from the microcontroller are received through this terminal.

$\overline{CS}$

This is the device Chip Select terminal of the serial peripheral interface. When this terminal is LOW, the internal serial peripheral interface of the device is selected.

$\overline{WDOG}$

The Watchdog terminal is used to signal that a software watchdog has not been properly triggered.

DEVICE OPERATION

Power Supply

The 33742 is supplied from the battery line through the V_{SUP} terminal. An external diode is required to protect against negative transients and reverse battery. The 33742 can operate from 4.5 VDC and under jump-start conditions at 27 VDC.

The V_{SUP} terminal sustains standard automotive voltage conditions such as load dump at 40 V. When V_{SUP} falls below 3.0 V typical, the 33742 detects it and stores the information in the Mode Control Register (MCR) bit BATFAIL. Detection is available in all operation modes.

Note For a detailed description of all the registers mentioned in this section, refer to the section titled SPI INTERFACE AND REGISTER DESCRIPTION beginning on page 38.

The 33742 incorporates a battery early warning function, which provides a maskable interrupt when the V_{SUP} voltage is below 6.0 V typical. A hysteresis is included. Operation is only in Normal and Standby modes. V_{SUP} LOW is reported in the Input/Output Register (IOR).

V_{DD} Regulator

The V_{DD} regulator is a 5.0 V output with output current capability up to 200 mA. It includes a voltage monitoring circuitry associated with an undervoltage reset function. The V_{DD} regulator is fully protected against overcurrent and short circuit. It has overtemperature detection warning flags (bit VDDTEMP in the MCR and INTR registers) and overtemperature shutdown with hysteresis.

V2 Regulator

V2 regulator circuitry is designed to drive an external pass transistor increasing output current flexibility. Two terminals, V2 and V2CTRL, are used to achieve the flexibility. Output voltage is 5.0 V and is realized by a tracking function of the V_{DD} regulator. The recommended ballast transistor is MJD32C. Other transistors can be used, however. Depending on the PNP transistor gain, an external resistor-capacitor network might be connected. V2 is the supply input for the CAN cell. The state of V2 is reported in the IOR register (bit V2LOW set to logic [1] if V2 is below 4.0 V typical).

HS V_{SUP} Switch Output

HS output is a 2.0 Ω typical switch from V_{SUP} terminal. It allows the supply of external switches and their associated pullup or pulldown circuitry, in conjunction, for example, with the wake-up input terminals L0:L3. Output current is limited to 200 mA and HS is protected against short circuit and has an overtemperature shutdown (bit HSOT in the IOR register and bit HSOT-V2LOW in the INTR register).

HS output is controlled by the bit HSON in the IOR register. Thanks to an internal timer, HS can be activated at regular intervals in Sleep and Stop modes. It can also be permanently turned on in Normal or Standby modes to drive loads or supply peripheral components. No internal clamping protection circuit is implemented; thus dedicated external protection circuitry is required in case of inductive load drive. HS negative voltage should not go below -0.3 V.

Battery Fail Early Warning

Refer to the discussion under the heading Power Supply, above.

Internal Clock

The 33742 has an internal clock used to generate all timings (reset, watchdog, cyclic wake-up, filtering time, etc.). Two oscillators are implemented. A high-accuracy (±12 percent) oscillator used in Normal Request, Normal, and Standby modes, and a low-accuracy (±30 percent) oscillator used in Sleep and Stop modes.

Functional Modes

The 33742 has four modes of operation, all controlled by the SPI. The modes are Standby, Normal, Stop, and Sleep. An additional temporary mode called Normal Request mode is automatically accessed by the device after reset or wake-up from Stop mode. A Reset mode is also implemented. Special modes and configuration are possible for debug and program microcontroller flash memory.

Table 2 below offers a summary of the functional modes.

Reset Mode

In the Reset mode, the $\overline{RST}$ terminal is LOW and a timer runs for t_{RSTDUR} time. After t_{RSTDUR} has elapsed, the 33742 enters Normal Request mode. Reset mode is entered if a reset condition occurs (V_{DD} LOW, watchdog timeout, or watchdog trigger in a closed window).

Normal Request Mode

Normal Request mode is a temporary mode automatically accessed by the 33742 after the Reset mode or after the 33742 wakes up from Stop mode. After wake-up from the Sleep mode or after device power-up, the 33742 enters the Reset mode before entering the Normal Request mode. After a wake-up from the Stop mode, the 33742 enters the Normal Request mode directly.

Table 2. Table of Operation

Mode	Voltage Regulator HS Switch	Wake-Up Capabilities (if Enabled)	$\overline{RST}$ Terminal	$\overline{INT}$ Terminal	Watchdog Software	CAN Cell
Normal Request	V_{DD}: ON, V2: OFF, HS: OFF	–	Low for t_{RSTDUR} time, then HIGH	–	–	–
Normal	V_{DD}: ON, V2: ON, HS: Controllable	–	Normally HIGH. Active LOW if $\overline{WDOG}$ or V_{DD} undervoltage occurs	If enabled, signal failure (V_{DD} Pre-Warning Temp, CAN, HS)	Running	TXD/RXD
Standby	V_{DD}: ON, V2: OFF, HS: Controllable	–	Same as Normal mode	Same as Normal mode	Running	Low power
Stop	V_{DD}: ON (Limited Current Capability), V2: OFF, HS:OFF or Cyclic Sense	CAN, SPI, L0:L3, Cyclic Sense, Forced Wake-Up, I_{DD} Overcurrent (Note 39)	Normally HIGH. Active LOW if $\overline{WDOG}$ (Note 40) or V_{DD} undervoltage occurs	Signal 33742 wake-up and $I_{DD} > I_{DDS-WU}$ (not maskable)	Running if enabled. Not running if disabled	Low power. Wake-up capability if enabled
Sleep	V_{DD}: OFF, V2: OFF, HS: OFF or Cyclic	CAN, SPI, L0:L3, Cyclic Sense Forced Wake-Up	LOW	Not Active	Not running	Low power. Wake-up capability if enabled
Normal Debug (Note 38)	Same as Normal	–	Normally HIGH. Active LOW if V_{DD} undervoltage occurs	Same as Normal	Not running	Same as Normal
Standby Debug (Note 38)	Same as Standby	–	Normally HIGH. Active LOW if V_{DD} undervoltage occurs	Same as Standby	Not running	Same as Standby
Stop Debug (Note 38)	Same as Stop	Same as Stop	Normally HIGH. Active LOW if V_{DD} undervoltage occurs	Same as Stop	Not running	Same as Stop
Flash Programming	Forced externally	–	Not operating	Not operating	Not operating	Not Operating

Notes

38. Mode entered via special sequence described under the heading Debug Mode: Hardware and Software Debug with the 33742 beginning on page 25.
39. I_{DD} overcurrent always enabled.
40. $\overline{WDOG}$ if enabled.

In Normal Request mode, the V_{DD} regulator is ON, the V2 regulator is OFF, and the $\overline{RST}$ terminal is HIGH. As soon as the 33742 enters the Normal Request mode, an internal 350 ms timer is started (parameter t_{NRTOUT}). During these 350 ms, the MCU of the application must address the 33742 via SPI and configure the TIM1 subregister to select the watchdog period. This is the condition for the 33742 to stop the 350 ms timer and go into the Normal or Standby mode and set the watchdog timer according to the configuration.

Normal Request Entered and No Watchdog Configuration Occurs

If the Normal Request mode is entered after the 33742 powers up or after a wake-up from Stop mode, and if no watchdog configuration occurs while the 33742 is in Normal Request mode, the 33742 goes into Reset mode after the 350 ms time period has expired before again going into Normal Request mode. If no watchdog configuration is achieved, the 33742 alternatively goes from Normal Request mode, to Reset mode, to Normal Request mode, and so on.

If the Normal Request mode is entered after a wake-up from Sleep mode, and if no watchdog configuration occurs while the 33742 is in Normal Request mode, the 33742 goes back to Sleep mode.

Normal Mode

In Normal mode, both the V_{DD} and V2 regulators are ON. This corresponds to the normal application operation. All functions are available in this mode (watchdog, wake-up input reading through SPI, HS activation, and CAN communication). Watchdog software is running and must be periodically cleared through SPI.

Standby Mode

In Standby mode, only the V_{DD}regulator is ON. The V2 regulator is turned OFF by disabling the V2CTRL terminal. The CAN interface is not able to send messages. If a CAN message is received, the CANWU bit is set. Other functions available are L0:L3 input reading through SPI and HS activation. Watchdog is running.

Sleep Mode

In Sleep mode, the V_{DD} and V2 regulators are OFF. Current from the V_{SUP} terminal is reduced. In Sleep mode, the 33742 can be awakened by L0:L3 inputs, by cyclic sense of the L0:L3 inputs, by the automatic forced wake-up timer, and from the CAN physical interface receiving an incoming CAN message. When a wake-up occurs, the 33742 goes first into the Reset mode before entering Normal Request mode.

Stop Mode

The V2 regulator is turned OFF by disabling the V2CTRL terminal. The V_{DD} regulator is activated in a special low power mode, allowing the delivery of a few mA. The objective is to maintain power on the MCU of the application while the MCU is turned into power-saving condition (i.e, Stop or Wait modes). In Stop mode, the device supply current from V_{PWR} is very low.

When the application is in Stop mode (both MCU and 33742), the application can wake up from either the 33742 side (for example, cyclic sense, forced wake-up, CAN message, wake-up inputs, and overcurrent on V_{DD}) or the MCU side (key wake-up, etc.).

Stop mode is always selected by SPI. In Stop mode, the watchdog software may be either running or not running depending upon selection by SPI (Reset Control Register [RCR], bit WDSTOP). To clear the watchdog if it is running, the 33742 must be awakened by the $\overline{CS}$ terminal (SPI wake-up). In Stop mode, the 33742 wake-up capability is identical to that in Sleep mode, with the addition of $\overline{CS}$ and V_{DD} overcurrent wake-up. Refer to Table 2, page 20.

Application Wake-Up from 33742 Side

When the application is in Stop mode, it can wake up from the 33742 side. When a wake-up is detected by the 33742 (for example, CAN, wake-up input), the 33742 turns itself into Normal Request mode and generates an interrupt pulse at the $\overline{INT}$ terminal.

Application Wake-Up from MCU Side

When the application is in Stop mode, the wake-up event may come from the MCU side. In this case the MCU signals to the 33742 by a LOW-to-HIGH transition on the $\overline{CS}$ terminal. Then the 33742 goes into Normal Request mode and generates an interrupt pulse at the $\overline{INT}$ terminal.

Stop Mode Current Monitor

If the V_{DD} output current exceeds an internal threshold ($I_{DDS\text{-}WU}$), the 33742 goes automatically into Normal Request mode and generates an interrupt at the $\overline{INT}$ terminal. The interrupt is not maskable and the INTR register will have no flag set.

Interrupt Generation When Wake-Up from Stop Mode

When the 33742 wakes up from Stop mode, it first enters the Normal Request mode before generating a pulse (10 µs typical) on the $\overline{INT}$ terminal. These interrupts are not maskable, and the wake-up event can be read through the SPI registers, CANWU bit in the CAN Register (CANR), and LCTRx bit in the Wake-Up Register (WUR). In case of wake-up from Stop mode overcurrent or from forced wake-up, no bit is set. After the $\overline{INT}$ pulse, the 33742 accepts SPI command after a time delay ($t_{S\text{-}1STSPI}$).

Watchdog Software in Stop Mode

If watchdog is enabled, the MCU has to wake up independently of the 33742 before the end of the 33742 watchdog time. In order to do this, the MCU must signal the wake-up to the 33742 through the SPI wake-up ($\overline{CS}$ activation). The 33742 then wakes up and jumps into the Normal Request mode. The MCU has to configure the 33742 to go to either Normal or Standby mode. The MCU can then decide to go back to the Stop mode.

If no MCU wake-up occurs within the watchdog timing the 33742 activates the $\overline{\text{RST}}$ terminal and jumps into the Normal Request mode. The MCU can then be initialized.

Stop Mode Enter Command

Stop mode is entered at the end of the SPI message at the rising edge of the $\overline{\text{CS}}$. (Refer to the t $_{\overline{\text{CS}}\text{-STOP}}$ data in the Dynamic Electrical Characteristics table on page 13.) Once Stop mode is entered, the 33742 can wake up from the V_{DD} regulator overcurrent detection. In order to allow time for the MCU to complete the last CPU instruction, allowing the MCU to enter its low power mode, a deglitcher time of 40 µs typical is implemented.

Figure 8, page 22, depicts the operation of entering the Stop mode.

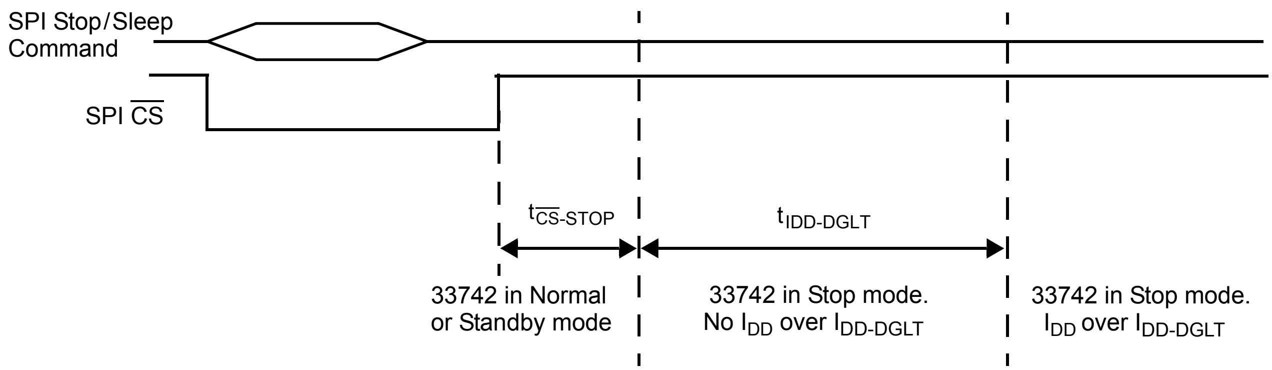


Figure 8. Entering Stop Mode

$\overline{\text{RST}}$ and $\overline{\text{WDOG}}$ Terminals, Software Watchdog Operations

Watchdog Software (Selectable Watchdog Window or Watchdog Timeout)

Watchdog software is used in the 33742 Normal and Standby modes for monitoring the MCU. Watchdog may be either watchdog window or watchdog timeout, selectable by SPI (TIM1 subregister, bit WDW). Default is watchdog window.

The watchdog period may be set from 10 ms to 350 ms (TIM1 subregister, bits WDT0 and WDT1). When watchdog window is selected, the closed window is the first part of the selected period, and the open window is the second part of the period. (Refer to Timing Register (TIM1/2) beginning on page 43.)

Watchdog can only be cleared within the open window time. Any attempt to clear watchdog in the closed window will generate a reset. Watchdog is cleared through SPI by addressing the TIM1 subregister.

$\overline{\text{RST}}$ Terminal Description

A reset output is available to reset the MCU. Causes of reset are the following:

- V_{DD} Falling Out of Range—If V_{DD} falls below the reset threshold ($V_{\overline{\text{RST}}\text{TH}}$), the $\overline{\text{RST}}$ terminal is pulled LOW until V_{DD} returns to the normal voltage.
- Power-ON Reset—At 33742 power-on or wake-up from Sleep mode, the $\overline{\text{RST}}$ terminal is maintained LOW until V_{DD} is within its operation range.
- Watchdog Timeout—If watchdog is not cleared, the 33742 will pull the $\overline{\text{RST}}$ terminal LOW for the duration of the reset time ($t_{\overline{\text{RST}}\text{DUR}}$).

Reset and Watchdog Operation

Table 3 describes watchdog and reset output modes of operation. $\overline{RST}$ is activated in the event V_{DD} fall or watchdog is not triggered. $\overline{WDOG}$ output is active LOW as soon as $\overline{RST}$ goes LOW and stays LOW as long as the watchdog is not properly reactivated by SPI. The $\overline{WDOG}$ output terminal is a push-pull structure that can drive external components of the application; for instance, to signal MCU wrong operation.

Figure 9 illustrates the device behavior in the event the TIM1 register in not properly accessed. In this case a software reset occurs, and the $\overline{WDOG}$ terminal is set LOW until the TIM1 register is properly accessed.

Table 3. Watchdog and Reset Output Operation

Events	$\overline{WDOG}$ Output	$\overline{RST}$ Output
Device Power-Up	LOW to HIGH	LOW to HIGH
V_{DD} Normal, Watchdog Properly Triggered	HIGH	HIGH
$V_{DD} < \overline{RST}_{TH}$	HIGH	LOW
Watchdog Timeout Reached	LOW (Note 41)	LOW

Notes
41. $\overline{WDOG}$ stays LOW until the TIM1 register is properly addressed through SPI.

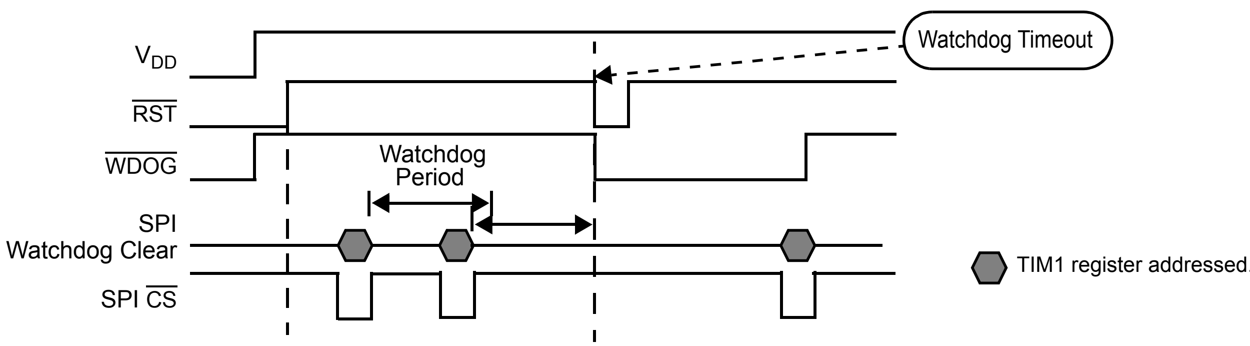


Figure 9. $\overline{RST}$ and $\overline{WDOG}$ Output Operation

Wake-Up Capabilities

Several wake-up capabilities are available to the 33742 when it is in Sleep or Stop mode. When a wake-up has occurred, the wake-up event is stored in the Wake-Up Register (WUR) or the CAN register. The MCU can then access the wake-up source. The wake-up options are selectable through SPI while the 33742 is in Normal or Standby mode and prior to entering low power mode (Sleep or Stop mode). When a wake-up occurs from Sleep mode, the 33742 activates V_{DD}. It generates an interrupt if wake-up occurs from Stop mode.

Wake-Up from Wake-Up Inputs (L0:L3) Without Cyclic Sense

The wake-up lines are dedicated to sense the state of external switches and if changes occur to wake up the MCU (in Sleep or Stop modes). Wake-up terminals L0:L3 are able to handle 40 VDC. The internal threshold is 3.0 V typical and these inputs can be used as an input port expander. The wake-up input states are read through SPI (WUR register).

In order to select and activate direct wake-up from the L0:L3 inputs, the WUR register must be configured with the appropriate level sensitivity. Additionally, the Low Power Control (LPC) Register must be configured with 0xx0 data (bits LX2HS and HSAUTO are set to 0).

Level sensitivity is selected by the WUR register. Level sensitivity is configured by L0:L3 input pairs: L0 and L1 level sensitivity are configured together, while L2 and L3 are configured together.

Cyclic Sense Wake-Up (Cyclic Sense Timer and Wake-Up Inputs L0:L3)

The 33742 can wake up upon state change of one of the four wake-up input lines (L0:L3) while the external pullup or pulldown resistor of the switches associated with the wake-up input lines are biased with HS V_{SUP} switch. The HS switch is activated in Sleep or Stop modes from an internal timer. Cyclic Sense and Forced Wake-Up are exclusive. If Cyclic Sense is enabled, Forced Wake-Up cannot be enabled.

In order to select and activate the cyclic sense wake-up from the L0:L3 inputs, the WUR register must be configured with the appropriate level sensitivity, and the LPC register must be configured with 1xx1 data (bit LX2HS set at 1 and bit HSAUTO set at 1). The wake-up mode selection (direct or cyclic sense) is valid for all four wake-up inputs.

Forced Wake-Up

The 33742 can wake up automatically after a predetermined time spent in Sleep or Stop mode. Cyclic Sense and Forced Wake-up are exclusive. If Forced Wake-Up is enabled (FWU bit set to 1 in the LPC register), Cyclic Sense cannot be enabled.

CAN Interface Wake-Up

The 33742 incorporates a high-speed 1.0 Mbps CAN physical interface. It is compatible with ISO 11898-2. The control of the CAN physical interface operation is accomplished through the SPI. CAN modes are independent of the 33742 operation modes.

The 33742 can wake up from a CAN message if the CAN wake-up is enabled. Refer to the section titled CAN BUS MODULE DESCRIPTION beginning on page 29 for details of the wake-up detection.

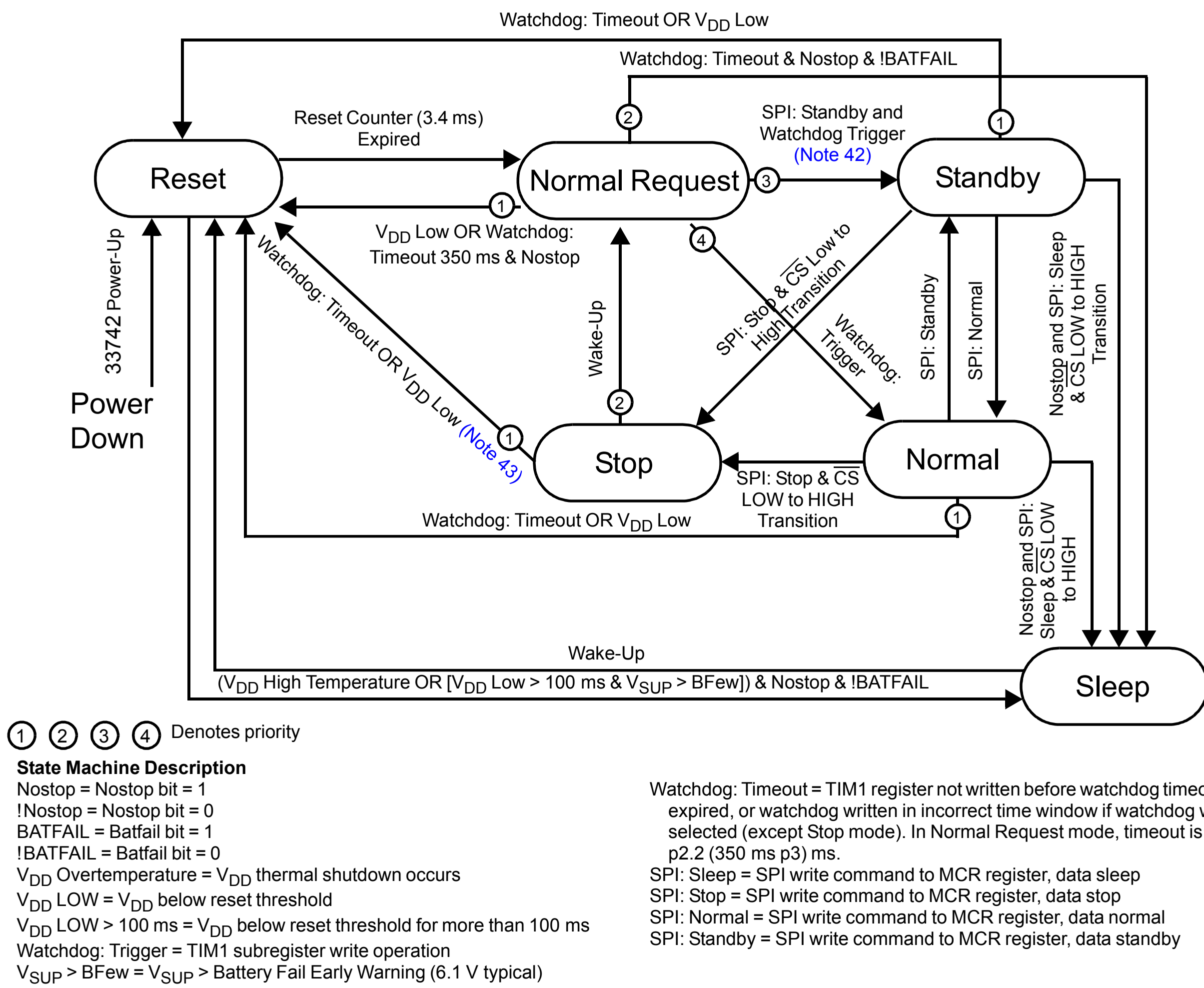
SPI Wake-Up

The 33742 can be awakened by the $\overline{CS}$ terminal in Sleep or Stop modes. Wake-up is detected by the $\overline{CS}$ terminal transition from LOW to HIGH level. In Stop mode, this corresponds with the condition where the MCU and the 33742 are in Stop mode and when the application wake-up event comes through the MCU.

33742 Power-Up and 33742 Wake-Up from Sleep Mode

After device or system power-up, or after the 33742 wakes up from Sleep mode, the 33742 enters into the Reset mode prior to moving into Normal Request mode.

Figure 10 shows the device state diagram and Figure 11, page 25, shows device behavior after power-up sequence.



Notes

42. These two SPI commands must be sent consecutively in this sequence.
43. If watchdog activated.

Figure 10. 33742 State Diagram (Not Valid in Debug Modes)

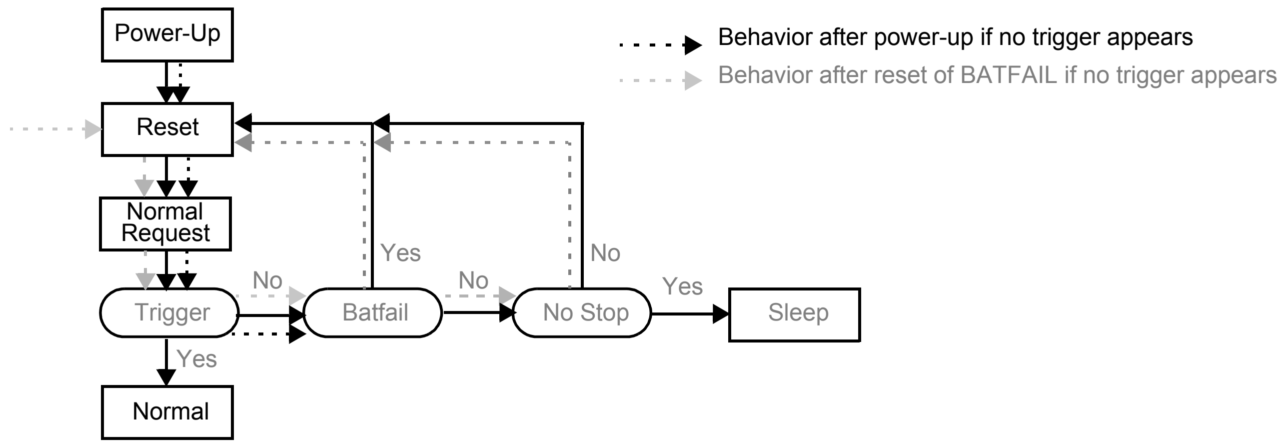


Figure 11. Behavior at 33742 Power-Up

Debug Mode: Hardware and Software Debug with the 33742

When the 33742 is mounted on the same printed circuit board as the MCU it supplies, both application software and 33742 dedicated routines must be debugged. The following features permit software debugging by allowing the possibility of disabling the 33742 internal software watchdog timer.

Device Power-Up, Reset Terminal Connected to V_{DD}

At 33742 power-up, V_{DD} voltage is provided; however, if no SPI communication occurs to configure the device, a reset occurs every 350 ms. In order to allow software debug and avoid MCU reset, the $\overline{RST}$ terminal can be connected directly to V_{DD} by a jumper.

Debug Modes with Software Watchdog Disabled Though SPI (Normal Debug, Standby Debug, and Stop Debug)

The watchdog software can be disabled through SPI. To avoid unwanted watchdog disable while limiting the risk of disabling the watchdog during 33742 normal operation, watchdog disable must be done using the following sequence:

- Step 1–Power down the 33742.
- Step 2–Power up the 33742. This sets the BATFAIL bit, allowing the 33742 to enter Normal Request mode.
- Step 3–Write to the TIM1 subregister to allow the 33742 to enter Normal mode.
- Step 4–Write to the MCR register with data 0000. This enables the debug mode. Complete SPI byte is 0001 0000.
- Step 5–Write to the MCR register normal debug. SPI byte is 0001 x101.

  Important While in debug mode, the 33742 can be used without having to clear the watchdog on a regular basis to facilitate software and hardware debug.

- Step 6–To leave the debug mode, write 0000 to the MCR register.

At Step 2, the 33742 is in Normal Request. Steps 3, 4, and 5 should be completed consecutively and within the 350 ms time period of the Normal Request mode. If not, the 33742 will go into Reset mode and enter Normal Request again.

Figure 12, page 26, illustrates debug mode selection.

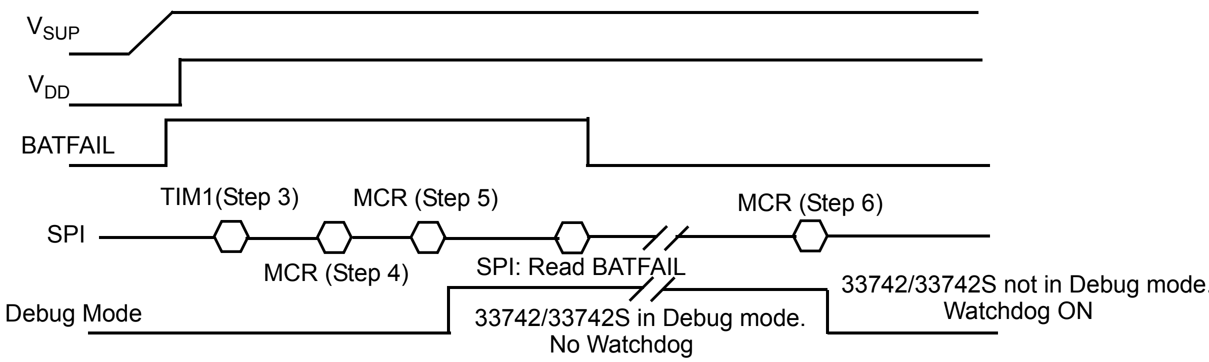


Figure 12. Entering Debug Mode

When the 33742 is in debug mode and has been set into Stop Debug or Sleep, a wake-up causes the 33742 to enter the Normal Request mode for 350 ms. To avoid having the 33742 generate a reset (enter Reset mode), the desired next debug mode (Normal Debug or Standby Debug) should be configured within the 350 ms time period of the Normal Request mode.

To avoid entering debug mode after a power-up, first read the BATFAIL bit (MCR read) and write 0000 into the MCR register.

Figure 13 below and Figure 14, page 27, show the detailed operation of the 33742 once the debug mode has been selected.

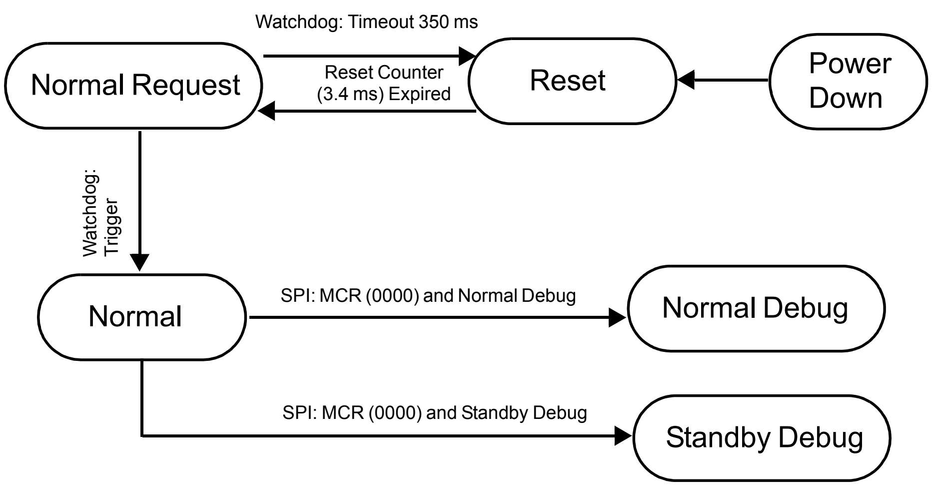
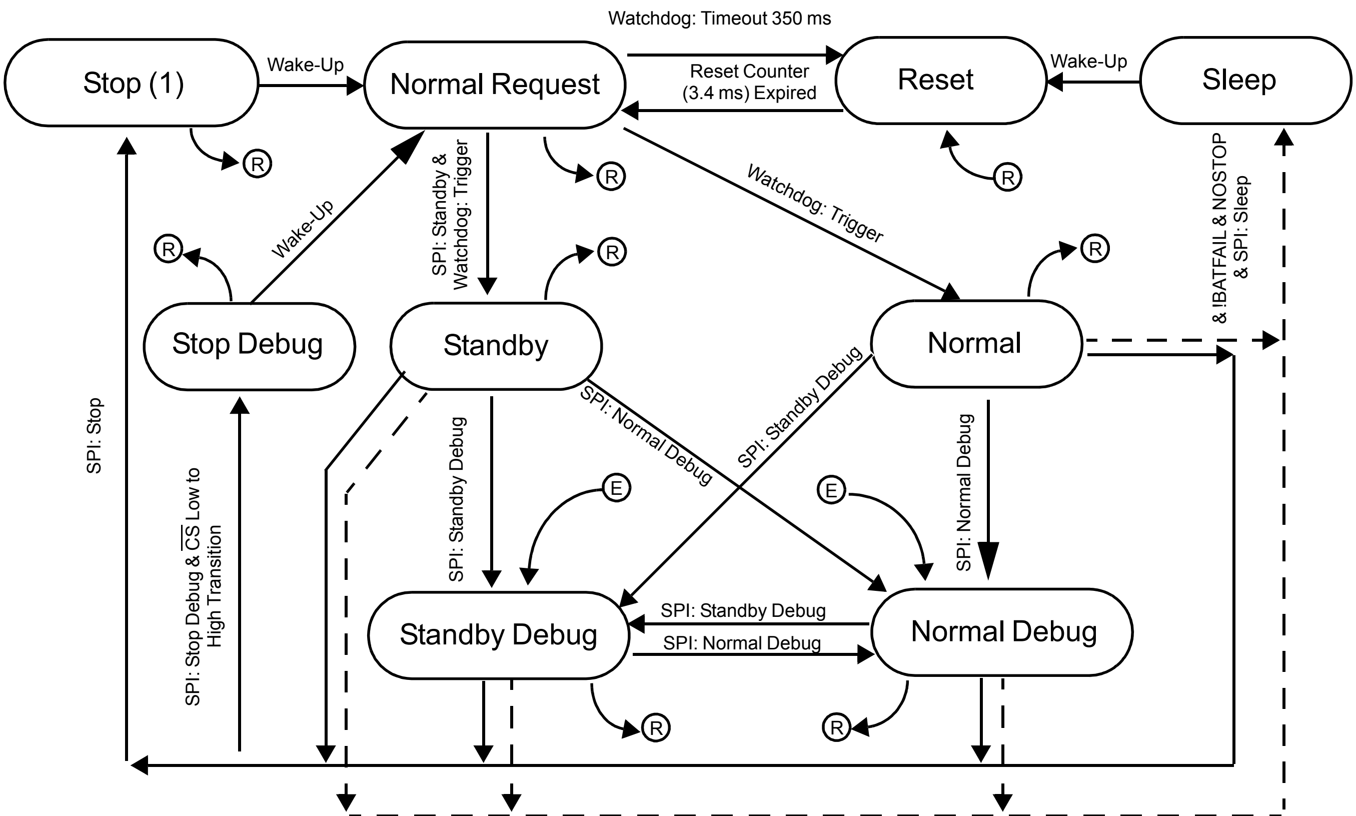


Figure 13. Transitions to Enter Debug Modes



(1) If Stop mode is entered, it is entered without watchdog, no matter the WDSTOP bit.
(E) Debug mode entry point (Step 5 of the Debug mode entering sequence).
(R) Represents transitions to Reset mode due to V_{DD} low.

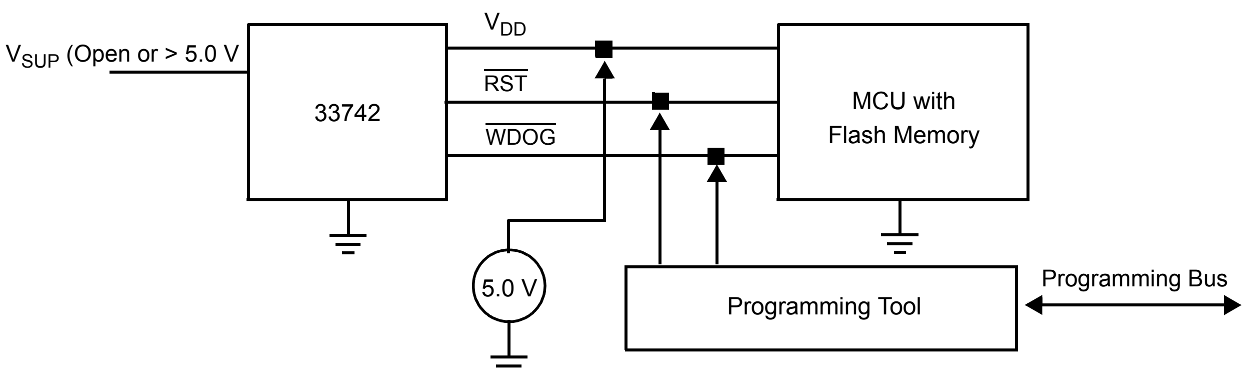
Figure 14. Simplified 33742 State Diagram in Debug Modes

MCU Flash Programming Configuration

To allow for the possibility of downloading software into the application memory (MCU EEPROM or Flash), the 33742 is capable of allowing (1) V_{DD} to be forced by an external power supply to 5.0 V and (2) the $\overline{RST}$ and the $\overline{WDOG}$ outputs to be forced by external signal sources to 0 V or 5.0 V, both without damaging the device. This allows, for example, the complete application board to be supplied by external power supply and external signal to be applied to the reset terminals. No functions of the 33742 are operating. Figure 15 illustrates a typical configuration for the connection of programming and debugging tools.

The V_{DD} regulator has an internal pass transistor between V_{SUP} and the V_{DD} output terminal. Biasing the V_{DD} output terminal with a voltage greater than V_{SUP} potential will force current through the body diode of the internal pass transistor to the V_{SUP} terminal. Therefore, V_{SUP} should be left open or forced to a value equal to or above V_{DD}.

The $\overline{RST}$ terminal is periodically pulled LOW for t_{RSTDUR} time (device in reset mode), before being pulled to V_{DD} for 350 ms typical (device in Normal Request mode). During the time reset is LOW, the $\overline{RST}$ terminal sinks 5.0 mA maximum (I_{PDW}).



Note External supply and sources applied to V_{DD}, $\overline{RST}$, and $\overline{WDOG}$ test points on application circuit board.

Figure 15. Simplified Schematic for Microcontroller Flash Programming

CAN BUS MODULE DESCRIPTION

Introduction

The 33742 features a high-speed CAN physical interface for bus communication between 60 kbps up to 1.0 Mbps. Figure 16 below is a simplified block diagram of the CAN interface of the 33742.

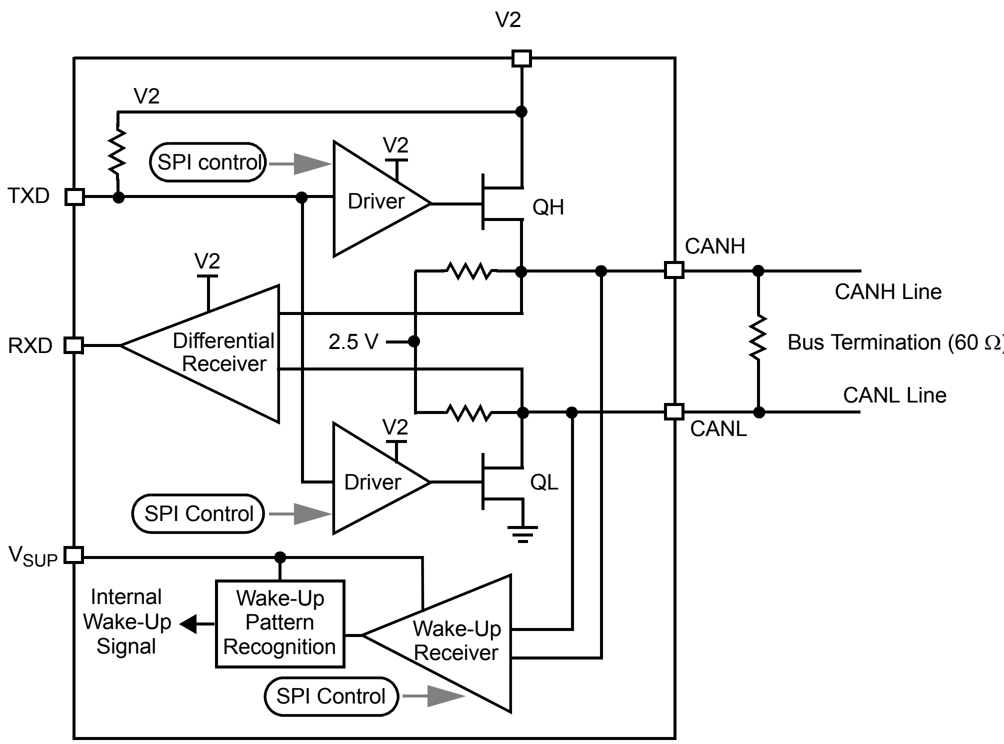


Figure 16. Simplified Block Diagram of CAN Interface

CAN Interface Supply

The supply voltage for the CAN driver is the V2 terminal. The CAN interface has also a supply path from the battery line, through the V_{SUP} terminal. This path is used in CAN Sleep mode to allow wake-up detection.

During CAN communication (transmission and reception), the CAN interface current is sourced from the V2 terminal. During CAN low power mode, the current is sourced from the V_{SUP} terminal.

Main Operation Modes Description

The CAN interface of the 33742 has two main operation modes: TXRX and Sleep mode. The modes are controlled by the CAN SPI Register. In the TXRX mode, which is used for communication, four different slew rates are available for the user. In the Sleep mode, the user has the option of enabling or disabling the remote CAN wake-up capability.

CAN Driver Operation in TXRX Mode

When the CAN interface of the 33742 is in TXRX mode, the driver has two states: recessive or dominant. The driver state is controlled by the TXD terminal. The bus state is reported through the RXD terminal.

When TXD is HIGH, the driver is set in recessive state, and CANH and CANL lines are biased to the voltage set at V2 divided by 2, or approximately. 2.5 V.

When TXD is LOW, the bus is set into dominant state: CAN L and CANH drivers are active. CANL is pulled to ground, and CANH is pulled HIGH toward 5.0 V (voltage at V2).

The RXD terminal reports the bus state: CANH minus CANL voltage is compared versus an internal threshold (a few hundred millivolts). If CANH minus CANL is below the threshold, the bus is recessive and RXD is set HIGH. If CANH minus CANL is above the threshold, the bus is dominant and RXD is set LOW. This is illustrated in Figure 16, page 29.

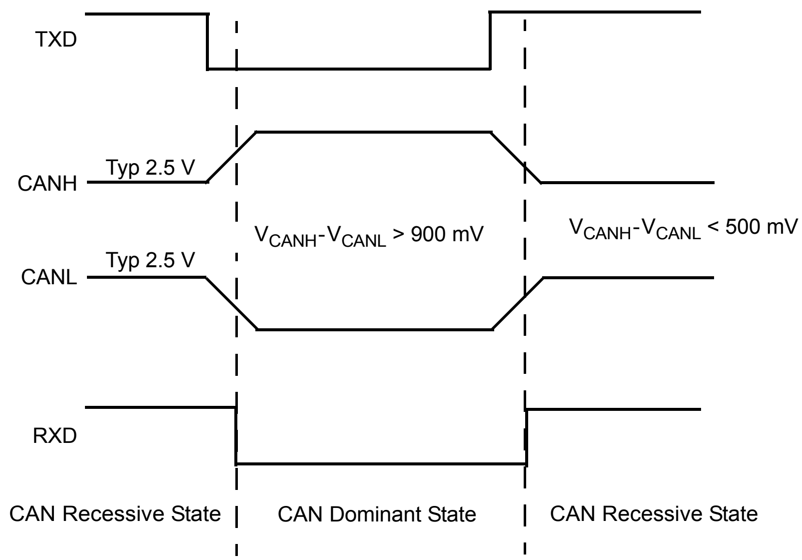


Figure 17. CAN Interface Levels

TXD and RXD Terminals

The TXD terminal has an internal pullup to V2. The state of TXD depends on the V2 status. RXD is a push-pull structure, supplied by V2. When V2 is set at 5.0 V and CAN is TXRX mode, RXD reports bus status. For details, refer to Table 2, page 20, Table 4, below, and Table 5, page 31.

CAN TXRX Mode and Slew Rate Selection

The slew rate selection is done via CAN register (refer to Tables 16 through 18 on page 40). Four slew rates are available, and controls the recessive to dominant and dominant to recessive transitions. The delay time from TXD terminal to CAN bus, from CAN bus to RXD and the TXD to RXD loop time is affected by the slew rate selection.

Table 4. CAN Interface/33742 Modes and Terminal Status—Operation with Ballast on V2 (Note 44)

Mode	CAN Mode (Controlled by SPI)	V2 Voltage	TXD Terminal	RXD Terminal	CANH/CANL (Disconnected from Other Node)	CAN Communication
Unpowered	–	0 V	LOW	LOW	Floating to GND	NO
Reset (with Ballast)	–	0 V	LOW	LOW	Floating to GND	NO
Normal Request (with Ballast)	–	0 V	LOW	LOW	Floating to GND	NO
Normal	Sleep	5.0 V	0 V	5.0 V	Floating to GND	NO
Normal	Normal Slew Rate 0, 1, 2, 3	5.0 V	Internal Pullup to V2	Report Bus State HIGH if Bus Recessive, LOW if dominant	Bus Recessive CANH = CANL = 2.5 V	YES
Standby with External Ballast	Normal or Sleep	0 V	LOW	LOW	Floating to GND	NO
Sleep	Sleep	0 V	LOW	LOW	Floating to GND	NO. Wake-up if enabled
Stop	Sleep	0 V	LOW	LOW	Floating to GND	NO. Wake-up if enabled

Notes

44. See also Figure 28, page 46.

Table 5. CAN Interface/33742 Modes and Terminal Status—Operation without Ballast on V2 (Note 45)

Mode	CAN Mode (Controlled by SPI)	V2 Voltage	TXD Terminal	RXD Terminal	CANH/CANL (Disconnected from Other Node)	CAN Communication
Unpowered	–	0 V	LOW	LOW	Floating to GND	NO
Reset (with Ballast)	–	0 V	LOW	LOW	Floating to GND	NO
Normal Request without Ballast. V2 Connected to V_{DD}	–	5.0 V	LOW	5.0 V	Floating to GND	NO
Standby without External Ballast, V2 connected to V_{DD}	Normal or Sleep	5.0 V	0 V	5.0 V	Floating to GND	NO
Normal without External Ballast. V2 Connected to V_{DD}	Normal Slew Rate 0, 1, 2,3	5.0 V	5.0 V	5.0 V	Bus Recessive CANH = CANL = 2.5 V	YES
Normal without External Ballast, V2 Connected to V_{DD}	Sleep	5.0 V	0 V	5.0 V	Floating to GND	NO
Sleep	Sleep	0 V	LOW	LOW	Floating to GND	NO. Wake-up if enabled
Stop	Sleep	0 V	LOW	LOW	Floating to GND	NO. Wake-up if enabled

Notes

45. See also Figure 29, page 47.

CAN Sleep Mode

The 33742 offers two CAN Sleep modes:

- Sleep mode with CAN wake-up enable: detection of incoming CAN message and SBC wake-up.
- Sleep mode with CAN wake-up disable: no detection of incoming CAN message.

The CAN Sleep mode is done via the CAN SPI register.

In CAN Sleep mode (with wake-up enable or disable), the CAN interface is internally supplied from the V_{SUP} terminal. The voltage at V2 terminal can be either 5.0 V or turned off. When the CAN is in Sleep mode, the current sourced from V2 is extremely low. In most cases the V2 voltage is off; however, the CAN can be placed into Sleep mode even with 5.0 V applied on V2.

In CAN Sleep mode, the CANH and CANL drivers are disabled, and the receiver is also disabled. CANH and CANL are high ohmic termination to ground.

CAN Signals in TXRX and Sleep Modes

When the CAN interface is set back into TXRX mode by an SPI command, CAN H and CANL are set in recessive level. This is illustrated in Figure 18.

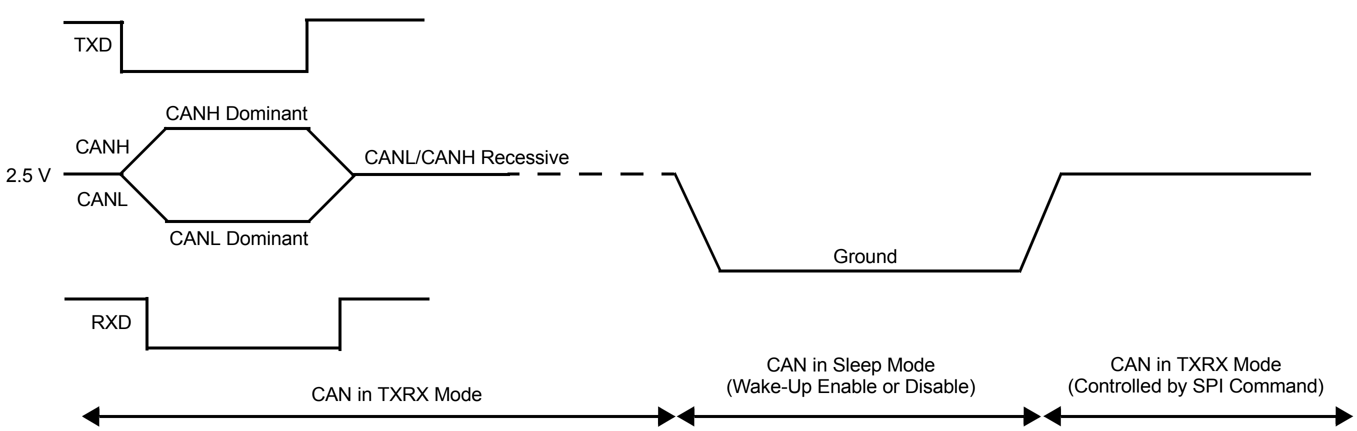


Figure 18. CAN Signals in TXRX and Sleep Modes

CAN in Sleep Mode with Wake-Up Enable

When the CAN interface is in Sleep mode with wake up enable, the CAN bus traffic is detected. The CAN bus wake up is a pattern wake up.

Pattern Wake-Up

In order to wake up the CAN interface, the following criteria must be fulfilled:

- The CAN interface wake-up receiver must receive a series of three consecutive valid dominant pulses, each of them has to be longer than 500 ns and shorter than 500 µs.
- The distance between 2 pulses must be lower than 500 µs.
- The three pulses must occur within a time frame of 1.0 ms.

The pattern wake-up of the 33742 CAN interface allow wake-up by any CAN message content.

Figure 19 below illustrates the CAN signals during a CAN bus Sleep state and wake-up sequence.

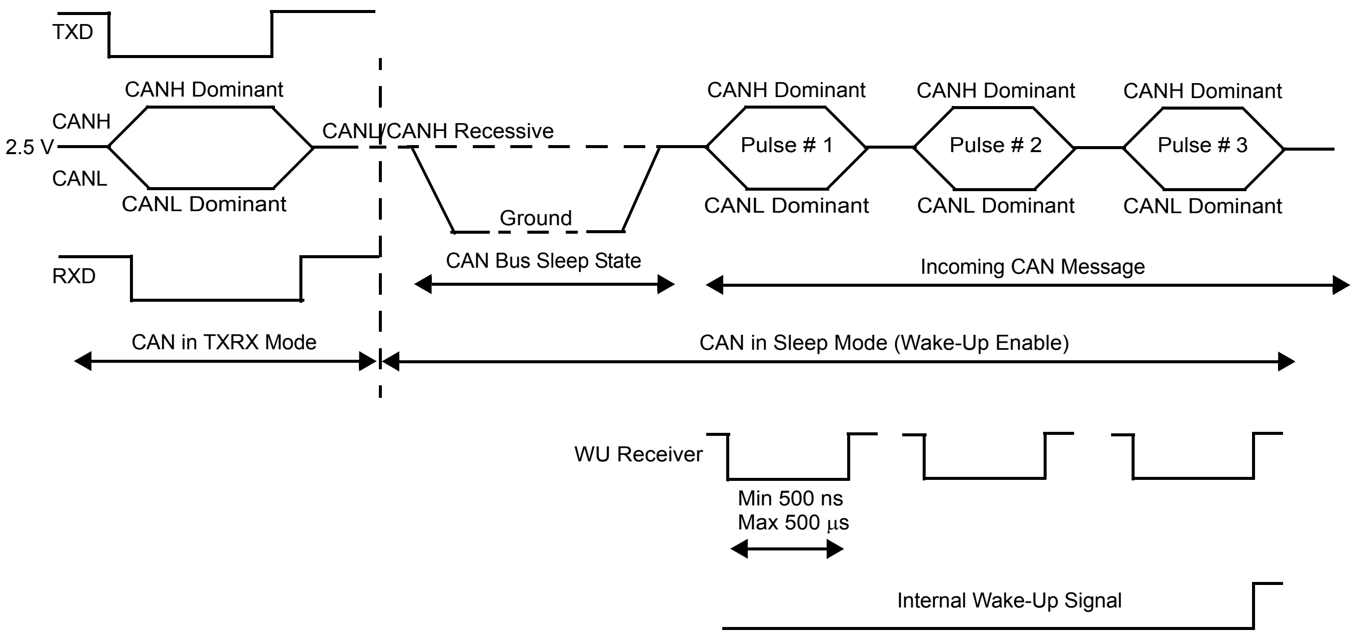


Figure 19. CAN Bus Signal During Can Sleep State and Wake-Up Sequence

Figure 20 illustrates how the wake-up signal is generated. First the CAN signal is detected by a low consumption receiver (WU receiver). Then the signal passes through a pulse width filter, which discards the undesired pulses. The pulse must have a width bigger than 0.5 µs and smaller than 500 µs to be accepted. When a pulse is discarded, the pulse counter is reset and no wake-up signal is generated. When a pulse is accepted, the pulse counter is incremented and, after three pulses, the internal wake-up signal is asserted.

Each one of the pulses must be spaced by no more than 500 µs. If not, the counter will be reset and no wake-up signal will be generated. This is accomplished by the wake-up timeout generator. The wake-up cycle is completed (and the wake-up flag reset) when the CAN interface is brought to CAN Normal mode.

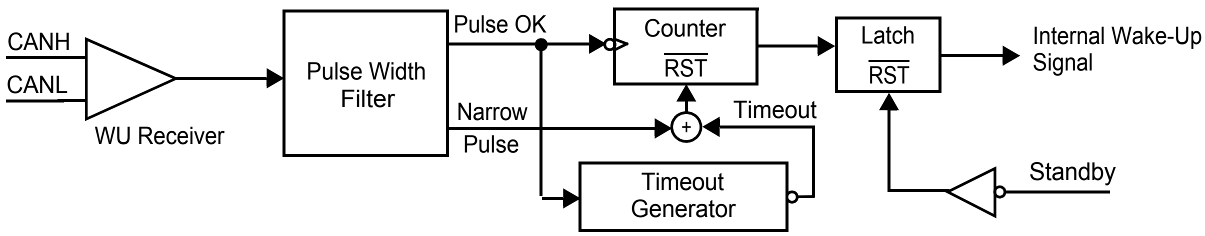


Figure 20. Wake-Up Functional Block Diagram

CAN Wake-Up Report

The CAN wake-up reports depend upon the 33742 low power mode.

If the 33742 is placed into Sleep mode (V_{DD} and V2 off), the CAN wake-up or any wake-up results in V_{DD} regulator turn on, leading to MCU supply turn on and reset release. If the 33742 is in Stop mode (V2 off and V_{DD} active), the CAN wake-up or any wake-up is signalled by a pulse on the INT output. In addition the CAN-WU bit is set in the CAN register.

If the 33742 is in Normal or Standby mode and the CAN interface is in Sleep mode with wake-up enable, the CAN wake-up is reported by the bit CANWU in the CAN register.

In the event the 33742 is in Normal mode and CAN Sleep mode with wake-up enable, it is recommended that the user check for the CAN WU bit prior to setting the 33742 in Sleep or Stop mode in case bus traffic has occurred while the CAN interface was in Sleep mode.

After CAN wake-up, a flag is set in the CAN register. Bit CAN-WU reports the CAN wake-up event while the 33742 was in Sleep or Stop mode. This bit is set until the CAN is in placed by SPI command into TXRX mode and the CAN register read.

CAN Bus Diagnostic

The 33742 can diagnose CANH or CANL lines short to GND, short to V_{SUP}, and short to V_{DD}.

As illustrated in Figure 21, several single-ended comparators are implemented on the CANH and CANL bus lines. These comparators monitor the bus level in recessive and dominant states. The information is then managed by a logic circuit to properly determine the failure and report it. Table 6 indicates the state of the comparators in the event of bus failure and the state of the drivers; that is, whether they are recessive or dominant.

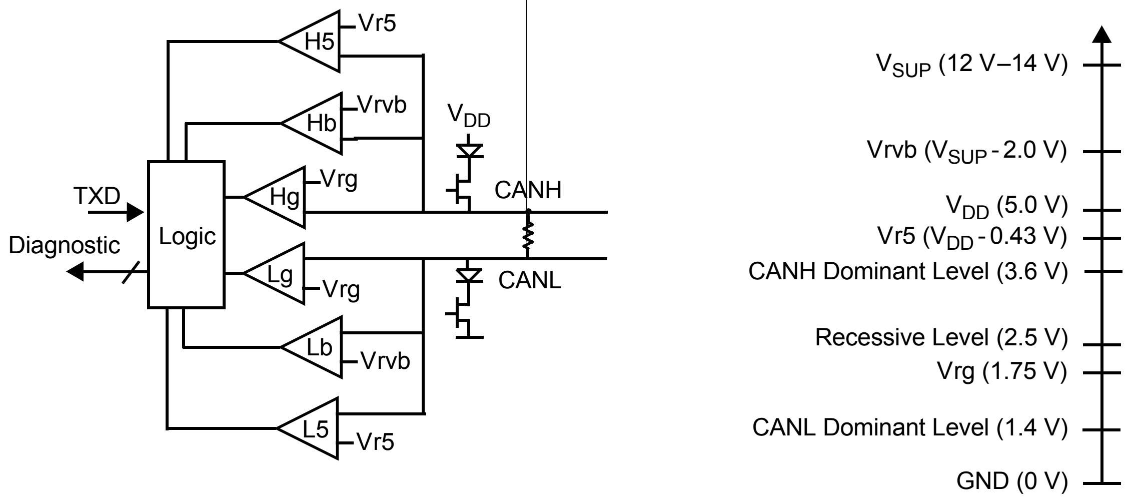


Figure 21. CAN Bus Simplified Structure

Table 6. Short to GND, Short to V_{SUP}, and Short to 5.0 V Detection Truth Table

Failure Description	Driver Recessive State		Driver Dominant State	
	Lg (Threshold 1.75 V)	Hg (Threshold 1.75 V)	Lg (Threshold 1.75 V)	Hg (Threshold 1.75 V)
No failure	1	1	0	1
CANL to GND	0	0	0	1
CANH to GND	0	0	0	0
	Lb (Threshold V_{SUP}-2.0 V)	Hb (Threshold V_{SUP}-2.0 V)	Lb (Threshold V_{SUP}-2.0 V)	Hb (Threshold V_{SUP}-2.0 [redacted]
No failure	0	0	0	0
CANL to V_{SUP}	1	1	1	1
CANH to V_{SUP}	1	1	0	1
	L5 (Threshold V_{DD}-0.43 V)	H5 (Threshold V_{DD}-0.43 V)	L5 (Threshold V_{DD}-0.43 V)	H5 (Threshold V_{DD}-0.43 [redacted]
No failure	0	0	0	0
CANL to V_{DD}	1	1	1	1
CANH to V_{DD}	1	1	0	1

Detection Principle

In the recessive state, if one of the two bus lines is shorted to GND, V_{DD}, or V_{SUP}, then voltage at the other line follows the shorted line due to bus termination resistance and the high impedance of the driver. For example, if CANL is shorted to GND, CANL voltage is zero, and CANH voltage, as measured by the Hg comparator, is also close to zero.

In the recessive state the failure detection to GND or V_{SUP} is possible. However, it is impossible to distinguish which bus line, CANL or CANH, is shorted to GND or V_{SUP}. In the dominant state, the complete diagnostic is possible once the driver is turned on.

CAN Bus Failure Reporting

CANL bus line failures (for example, CANL short to GND) is reported in the SPI register TIM1/2. CANH bus line (for example, CANH short to V_{SUP}) is reported in the LPC register.

In addition CANF and CAN-UF bits in the CAN register indicate that a CAN bus failure has been detected.

Non-Identified and Fully Identified Bus Failures

As indicated in Table 6, page 34, when the bus is in a recessive state it is possible to detect an error condition; however, is it not possible to fully identify which error. This is called "non-identified" or "under-acquisition" bus failure. If there is no communication (i.e., bus idle), it is still possible to warn the MCU that the device has started to detect a bus failure.

In the CAN register, bits D2 and D1 (CAN-F and CAN-UF, respectively) are used to signal bus failure. Bit D2 reports a bus failure and bit D1 indicates if the failure is identified or not (bit D1 is set to 1 if the error is not identified).

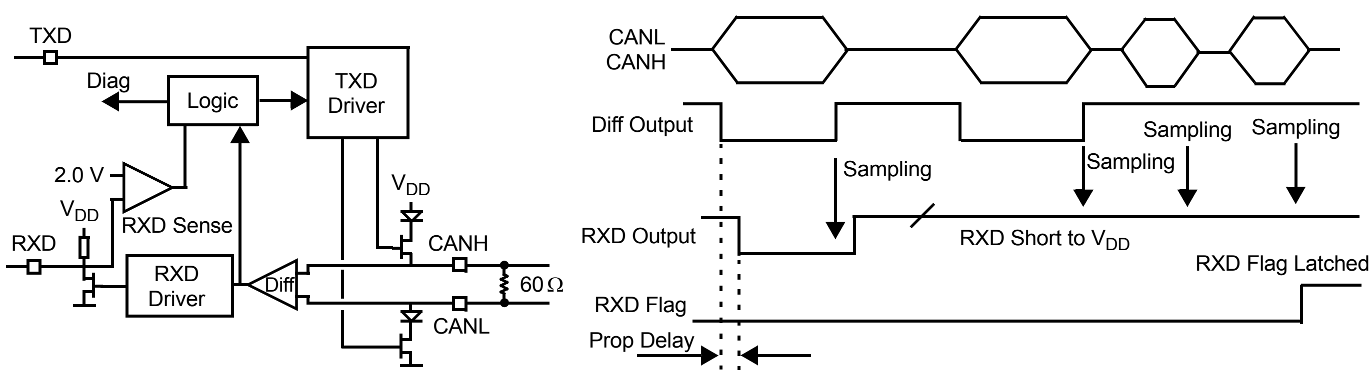
When the detection mechanism is complete, the error will be fully detected and reported in the TIM1/2 and LPC registers and bit D1 will be reset to 0.

Number of Samples for Proper Failure Detection

The failure detector requires at least one cycle of recessive and dominant state to properly recognize the bus failure. The error will be fully detected after five cycles of recessive-dominant states. As long as the failure detection circuitry has not detected the same error for five recessive-dominant cycles, the bit "non-identified failure" (CAN-UF) will be set.

RXD Permanent Recessive Failure

The purpose of this detection mechanism is to diagnose an external hardware failure at the RXD output terminal and to ensure that a permanent failure at the RXD terminal does not disturb network communication. In the event RXD is shorted to a permanent high level signal (i.e., 5.0 V), the CAN protocol module within the MCU cannot receive any incoming message. Additionally, the CAN protocol module cannot distinguish the bus idle state and could start communication at any time. To prevent this, an RXD failure detection, as illustrated in Figure 22 and explained below, is necessary.



Note RXD Flag is neither the RXPR bit in the LPC register nor the CAN-F bit in the INTR register.

Figure 22. RXD Path and RXD Permanent Recessive Detection Principle

RXD Failure Detection

The 33742 senses the RXD output voltage at each LOW-to-HIGH transition of the differential receiver. Excluding internal propagation delay, RXD output should be LOW when the differential receiver is LOW. In the event RXD is shorted to 5.0 V (e.g., to V_{DD}), RXD will be tied to a high level and the RXD short to 5.0 V can be detected at the next LOW-to-HIGH transition of the differential receiver. Compete detection requires three samples.

When the error is detected, the flag is latched and the CAN driver is disabled. The error is reported through the SPI register LPC, bit RXPR.

Recovery Condition

The internal recovery is completed by the sampling of a correct low level at TXD, as illustrated in Figure 23, page 36.

As soon as the RXD permanent recessive is detected, the RXD driver is deactivated and a weak pulldown current source is activated in order to allow recovery conditions. The driver stays disabled until the failure is cleared (RXD no longer permanent recessive) and the bus driver is activated by an SPI register command (write 1 to the CANCLR bit in the CAN register).

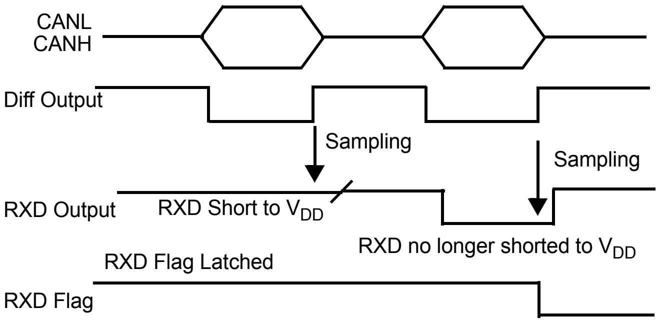


Figure 23. RXD Recovery Conditions

TXD Permanent Dominant Failure

Principle

In the event TXD is set to a permanent low level, the CAN bus is set into dominant level, and no communication is possible. The 33742 has a TXD permanent timeout detector. After timeout, the bus driver is disabled and the bus is released in a recessive state. The TXD permanent dominant failure is reported in the TIM1 register.

Recovery

The TXD permanent dominant is used and activated also in case of TXD short to RXD. The recovery condition for TXD permanent dominant (recovery means the reactivation of the CAN drivers) is done by an SPI command and is controlled by the MCU.

The driver stays disabled until the failure is cleared (TXD no longer permanent dominant) and the bus driver is activated by an SPI register command (write 1 to bit CANCLR in the CAN register).

TXD to RXD Short Circuit Failure

Principle

In the event TXD is shorted to RXD when an incoming CAN message is received, RXD is set LOW. Consequently, the TXD terminal is LOW and drives CANH and CANL into the dominant state. The bus is stuck in dominant and no further communication is possible.

Detection and Recovery

The TXD permanent dominant timeout will be activated and release the CANL and CANH drivers. However, at the next incoming dominant bit, the bus will then be stuck again in dominant. In order to avoid this situation, the recovery of the failure (recovery means the reactivation of the CAN drivers) is done by an SPI command and controlled by the MCU.

Internal Error Output Flags

There are internal error flags to signal whenever thermal protection is activated or overcurrent detection occurs on the CANL or CANH terminals (bit THERM-CUR). The errors are reported in the CAN register.

DEVICE FAULT OPERATION

Table 7 describes the relationship between device fault or warning and the operation of the V_{DD}, V2, CAN, and HS interface.

Table 7. Fault/Warning

Fault/Warning	V_{DD}	V2	CAN	HS
Battery Fail	Turn OFF	Turn OFF	Turn OFF due to V2. No communication	OFF
V_{DD} Temperature Prewarning	Warning flag only. Leave as is	No change	No change	No change
V_{DD} Overtemperature	Turn OFF	Turn OFF	Turn OFF due to V2. No communication	OFF
V_{DD} Overcurrent	V_{DD} regulator enters linear mode. V_{DD} undervoltage reset may occurs. V_{DD} overtemperature prewarning or shutdown may occur	Turn OFF if V_{DD} undervoltage reset occurs	If V2 is OFF, turn OFF and no communication	Turn OFF if V_{DD} undervoltage reset occurs
V_{DD} Short Circuit	V_{DD} undervoltage reset occurs. V_{DD} overtemperature prewarning or shutdown may occur	Turn OFF	Turn OFF due to V2. No communication	OFF
Watchdog Reset	ON	Turn OFF	Turn OFF due to V2. No communication	OFF
V2LOW (e.g., V2 < 4.0 V)	No change	V2 out of range	Turn OFF due to V2 low	No change
HS Overtemperature	No change	No change	No change	OFF
HS Overcurrent	No change	No change	No change	HS overtemperature may occur
V_{SUP} LOW	No change	No change	No change	No change
CAN Overtemperature	No change	No change	Disable. As soon as temperature falls, CAN is re-enabled automatically	No change
CAN Overcurrent	No change	No change	(Note 46)	No change
CANH Short to GND	No change	No change (Note 47)	No communication (Note 48)	No change
CANH Short to V_{DD}	No change	No change	Communication OK	No change
CANH Short to V_{SUP}	No change	No change	Communication OK	No change
CANL Short to GND	No change	No change	Communication OK	No change
CANL Short to V_{DD}	No change	No change	No communication (Note 48)	No change
CANL Short to V_{SUP}	No change	No change	No communication (Note 48)	No change

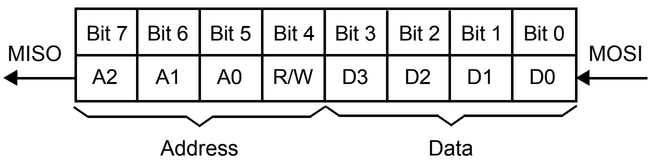
Notes

46. Refer to descriptions of CANH and CANL short to GND, V_{DD}, and V_{SUP} elsewhere in table.
47. Peak current 150 mA during TXD dominant only. Due to loss of communication, CAN controller reaches bus OFF state. Average current out of V2 is below 10 mA.
48. Overcurrent might be detected. Bit THERM-CUR set in CAN register.

Data Format Description

Figure 24 illustrates a register, an 8-bit SPI. The first three bits are used to identify the internal 33742 register address. Bit 4 is a read/write bit. The last four bits are data sent from the MCU to the 33742 or read back from the 33742 to the MCU.

The state of the MISO has no significance during the write operation. However, during the read operation the final four bits of MISO have meaning; namely, they contain the content of the accessed register.



Note Read operation: R/W bit = 0; Write operation: R/W = 1.

Figure 24. Data Format Description

Table 8 lists the possible reset conditions.

Table 8. Possible Reset Conditions

Condition	Name	Definition
33742 Reset	POR	Power-ON Reset
33742 Mode Transition	NR2R	Normal Request to Reset Mode
	NR2N	Normal Request to Normal Mode
	NR2STB	Normal Request to Standby Mode
	N2R	Normal to Reset Mode
	STB2R	Standby to Reset Mode
	STO2R	Stop to Reset Mode
	STO2NR	Stop to Normal Request
33742 Mode	RESET	33742 in Reset Mode

Register Descriptions

The following tables in this section describe the SPI register list and register bit meaning. Register reset value is also described, along with the reset condition. Reset condition is the condition causing the bit to be set at the reset value.

Table 9. List of Registers

Register	Address	Formal Name and Link	Comment and Use	
			Write	Read
MCR	$000	Mode Control Register (MCR) on page 39	Selection for Normal, Standby, Sleep, Stop, and Debug modes	BATFAIL, general failure, V_{DD} pre-warning, and Watchdog flag
RCR	$001	Reset Control Register (RCR) on page 40	Configuration for reset voltage level, CAN Sleep and Stop modes	
CAN	$010	CAN Register (CAN) on page 40	CAN slew rate, Sleep and Wake-Up enable/disable modes, drive enable after failure	CAN wake-up and CAN failure status bits
IOR	$011	Input/Output Register (IOR) on page 41	HS (High Side switch) control in Normal and Standby mode	HS overtemperature bit, V_{SUP}, and V2 Low status
WUR	$100	Wake-Up Register (WUR) on page 42	Control of wake-up input polarity	Wake-up input and real time Lx input state
TIM	$101	Timing Register (TIM1/2) on page 43	• TIM1: Watchdog timing control, Watchdog Window (WDW) or Watchdog Timeout (WTO) mode • TIM2: Cyclic Sense and Forced Wake-Up timing selection	CANL and TXD failure reporting
LPC	$110	Low Power Control Register (LPC) on page 44	Control HS periodic activation in Sleep and Stop modes, Forced Wake-Up mode activation, CAN-INT mode selection	CANH and RXD failure reporting
INTR	$111	Interrupt Register (INTR) on page 45	Enable or Disable of Interrupts	Interrupt source

Mode Control Register (MCR)

Tables 10 through 12 describe various Mode Control Register information.

Table 10. Mode Control Register

MCR	R/W	D3	D2	D1	D0
$000b	W	–	MCTR2	MCTR1	MCTR0
	R	BATFAIL (Note 49)	VDDTEMP	GFAIL	WDRST
Reset Value	–	–	0	0	0
Reset Condition (Write) (Note 50)	–	–	POR, RESET	POR, RESET	POR, RESET

Notes

49. BATFAIL bit cannot be set by SPI. BATFAIL is set when V_{SUP} falls below 3.0 V.
50. See Table 8, page 38, for definitions of reset conditions.

Table 11. Mode Control Register Control Bits

MCTR2	MCTR 1	MCTR 0	33742 Mode	Description
0	0	0	Enter/Exit Debug Mode	To enter/exit Debug Mode, refer to detailed description in Debug Mode: Hardware and Software Debug with the 33742, page 25.
0	0	1	Normal	–
0	1	0	Standby	–
0	1	1	Stop, Watchdog OFF (Note 51)	–
0	1	1	Stop, Watchdog ON (Note 51)	–
1	0	0	Sleep (Note 52)	–
1	0	1	Normal	No Watchdog running. Debug Mode.
1	1	0	Standby	
1	1	1	Stop	

Notes

51. Watchdog ON or OFF depends on RCR bit D3.
52. Before entering Sleep mode, bit BATFAIL in MCR must be previously cleared (MCR read operation), and bit NOSTOP in RCR must be previously set to 1.

Table 12. Mode Control Register Status Bits

Name	Value	Description
BATFAIL	0	V_{SUP} was not below V_{BF}.
	1	V_{SUP} has been below V_{BF}.
VDDTEMP	0	No overtemperature pre-warning.
	1	Temperature pre-warning on V_{DD} regulator (bit latched).
GFAIL	0	No failure.
	1	CAN Failure or HS overtemperature or V2 low.
WDRST	0	No watchdog reset occurred.
	1	Watchdog reset occurred.

Reset Control Register (RCR)

Tables 13 and 14 contain various Reset Control Register information.

Table 13. Reset Control Register

RCR	R/W	D3	D2	D1	D0
$001b	W	WDSTOP	NOSTOP	CAN SLEEP	RSTTH
	R				
Reset Value	–	1	0	0	0
Reset Condition (Write) (Note 53)	–	POR, RESET, STO2NR	POR, NR2N, NR2STB	POR, NR2N, NR2STB	POR

Notes

53. See Table 8, page 38, for definitions of reset conditions.

Table 14. Reset Control Register Control Bits

Name	Value	Description
WDSTOP	0	No Watchdog in Stop Mode.
	1	Watchdog runs in Stop Mode.
NOSTOP	0	Device cannot enter Sleep Mode.
	1	Sleep mode allowed. Device can enter Sleep Mode.
CAN SLEEP	0	CAN Sleep Mode disable (despite D0 bit in CAN register).
	1	CAN Sleep Mode enabled (in addition to D0 in CAN register).
RSTTH	0	Reset Threshold 1 selected (typ 4.6 V).
	1	Reset Threshold 2 selected (typ 4.2 V).

CAN Register (CAN)

Tables 15 through 18 contain various CAN register information. Table 15 describes control of the high-speed CAN module, mode, slew rate, and wake-up.

Table 15. CAN Register

CAN	R/W	D3	D2	D1	D0
$010b	W	CANCLR	SC1	SC0	MODE
	R	CANWU	CAN-F	CAN-UF	THERM-CUR
Reset Value	–	0	0	0	1
Reset Condition (Write) (Note 54)	–	POR	POR	POR	NR2N, STB2N

Notes

54. See Table 8, page 38, for definitions of reset conditions.

Table 16. CANCLR Control Bits

Value	Description
0	No effect.
1	Re-enables CAN driver after TXD permanent dominant or RXD permanent recessive failure occurred. Failure recovery conditions must occur to re-enable.

High-Speed CAN Transceiver Modes

The MODE bit (D0) controls the state of the CAN interface, TXRX or Sleep mode (Table 17). SC0 bit (D1) defines the slew rate when the CAN module is in TXRX, and it controls the wake-up option (wake-up enable or disable) when the CAN module is in Sleep mode.

Table 17. CAN High-Speed Transceiver Modes

SC1	SC0	MODE	CAN Mode (Pass 1.1)
0	0	0	CAN TXRX, Slew Rate 0
0	1	0	CAN TXRX, Slew Rate 1
1	0	0	CAN TXRX, Slew Rate 2

Table 18. CAN Register Status Bits

Name	Value	Description
CANWU	0	No CAN wake-up occurred.
	1	CAN wake-up occurred.
CAN-F	0	No CAN failure.
	1	CAN failure (Note 55).
CAN-UF	0	Identified CAN failure (Note 55).
	1	Non-identified CAN failure.
THERM-CUR	0	No overtemperature or overcurrent on CANH or CANL drivers.
	1	Overtemperature or overcurrent on CANH or CANL drivers.

Notes
55. Error bits are latched in the CAN register.

Input/Output Register (IOR)

Tables 19 through 21 contain various Input/Output Register information. Table 20 provides information about HS control in Normal and Standby modes, while Table 21 provides status bit information.

Table 19. Input/Output Register

IOR	R/W	D3	D2	D1	D0
$011b	W	–	HSON	–	–
	R	V2LOW	HSOT	VSUPLOW	DEBUG
Reset Value	–	–	0	–	–
Reset Condition (Write) (Note 56)	–	–	POR	–	–

Notes
56. See Table 8, page 38, for definitions of reset conditions.

Table 20. HSON Control Bits

Value	HS State
0	HS OFF, in Normal and Standby modes.
1	HS ON, in Normal and Standby modes (Note 57).

Notes
57. When HS is turned OFF due to an overtemperature condition, it can be turned ON again by setting the appropriate control bit to 1. Error bits are latched in the IOR register.

Table 21. Input/Output Register Status Bits

Name	Value	Description
V2LOW	0	V2 > 4.0 V.
	1	V2 < 4.0 V.
HSOT	0	No HS overtemperature.
	1	HS overtemperature.
VSUPLOW	0	V_{SUP} > 6.1 V.
	1	V_{SUP} < 6.1 V.
DEBUG	0	33742 not in Debug mode.
	1	33742 accepts command to go to Debug modes (no Watchdog).

Wake-Up Register (WUR)

Tables 22 through 24 contain various Wake-Up Register information. Local wake-up inputs L0:L3 can be used in both Normal and Standby modes as port expander, as well as for waking up the 33742 from Sleep or Stop modes (Table 22).

Table 22. Wake-Up Register

WUR	R/W	D3	D2	D1	D0
$100b	W	LCTR3	LCTR2	LCTR1	LCTR0
	R	L3WU	L2WU	L1WU	L0WU
Reset Value	–	0	0	0	0
Reset Condition (Write) (Note 58)	–	POR, NR2R, N2R, STB2R, STO2R			

Notes

58. See Table 8, page 38, for definitions of reset conditions.

Wake-up inputs can be configured by pair. L0 and L1 can be configured together, and L2 and L3 can be configured together (Table 23).

Table 23. Wake-Up Register Control Bits

LCTR3	LCTR2	LCTR1	LCTR0	L0:L1 Config	L2:L3 Config
x	x	0	0	Inputs Disabled	–
x	x	0	1	High Level Sensitive	
x	x	1	0	Low Level Sensitive	
x	x	1	1	Both Level Sensitive	
0	0	x	x	–	Inputs Disabled
0	1	x	x		High Level Sensitive
1	0	x	x		Low Level Sensitive
1	1	x	x		Both Level Sensitive

x = Don't care.

Table 24. Wake-Up Register Status Bits (Note 59)

Name	Value	Description
L3WU	0 or 1	If bit = 1, wake-up occurred from Sleep or Stop modes; if bit = 0, no wake-up has occurred. When device is in Normal or Standby mode, bit reports the State on Lx terminal (LOW or HIGH) (0 = Lx LOW, 1 = Lx HIGH)
L2WU	0 or 1	
L1WU	0 or 1	
L0WU	0 or 1	

Notes

59. WUR status bits have two functions. After 33742 wake-up, they indicate the wake up source; for example, L2WU set at 1 if wake-up source is L2 input. After 33742 wake-up and once the WUR register has been read, status bits indicate the real-time state of the Lx inputs (1 = Lx is above threshold, 0 = Lx input is below threshold). If after a wake-up from Lx input a watchdog timeout occurs before the first reading of the WUR register, the LxWU bits are reset. This can occur only if the 33742 was in Stop Mode.

Timing Register (TIM1/2)

Tables 25 through 29 contain various Timing Register information. The TIM register is composed of two subregisters:

1. TIM1—Controls the watchdog timing selection as well as either the watchdog window or the watchdog timeout option (Figure 25 and Figure 26, respectively). TIM1 is selected when bit D3 is 0 (Table 25). Watchdog timing characteristics are described in Table 26.
2. TIM2—Selects an appropriate timing for sensing the wake-up circuitry or cyclically supplying devices by switching the HS on or off. TIM2 is selected when bit D3 is 1 (Table 27). Figure 27, page 44, describes HS operation when cyclic sense is selected. Cyclic sense timing characteristics are described in Table 29, page 44.

Both subregisters also report the CANL and TXD diagnostic.

Table 25. TIM1 Timing and CANL Failure Diagnostic Register

TIM1	R/W	D3	D2	D1	D0
$101b	W	0	WDW	WDT1	WDT0
	R	CANL2VDD	CANL2BAT	CANL2GND	TXPD
Reset Value	–	–	0	0	0
Reset Condition (Write) (Note 60)	–	–	POR, RESET	POR, RESET	POR, RESET

Notes
60. See Table 8, page 38, for definitions of reset conditions.

Table 26. TIM1 Control Bits

WDW	WDT1	WDT0	Timing (ms typ)	Parameter	Description
0	0	0	9.75	Watchdog Period 1	No Window Watchdog
0	0	1	45	Watchdog Period 2	
0	1	0	100	Watchdog Period 3	
0	1	1	350	Watchdog Period 4	
1	0	0	9.75	Watchdog Period 1	Watchdog Window enabled (Window length is half the Watchdog Timing).
1	0	1	45	Watchdog Period 2	
1	1	0	100	Watchdog Period 3	
1	1	1	350	Watchdog Period 4	

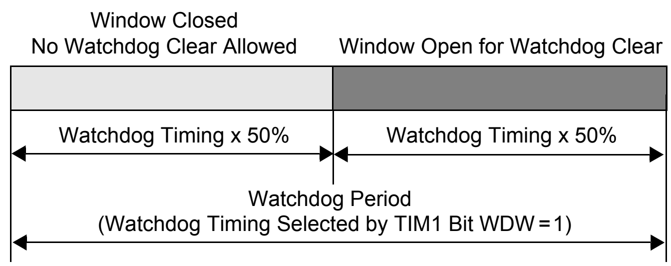


Figure 25. Window Watchdog

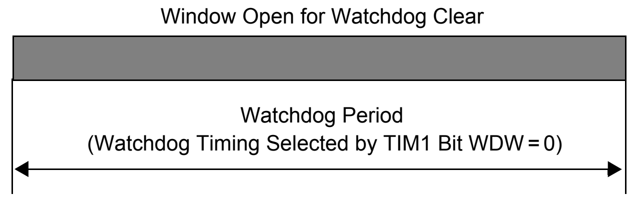


Figure 26. Timeout Watchdog

Table 27. Timing Register Status Bits

Name	Value	Failure Description
CANL2VDD	0	No CANL short to V_{DD}.
	1	CANL short to V_{DD}.
CANL2BAT	0	No CANL short to V_{SUP}.
	1	CANL short to V_{SUP}.
CANL2GND	0	No CANL short to GND.
	1	CANL short to GND.
TXPD	0	No TXD dominant
	1	TXD dominant.

Table 28. TIM2 Timing and CANL Failure Diagnostic Register

TIM2	R/W	D3	D2	D1	D0
$101b	W	1	CSP2	CSP1	CSP0
	R	CANL2VDD	CANL2BAT	CANL2GND	TXPD
Reset Value	–	–	0	0	0
Reset Condition (Write) (Note 61)	–	–	POR, RESET	POR, RESET	POR, RESET

Notes
61. See Table 8, page 38, for definitions of reset conditions.

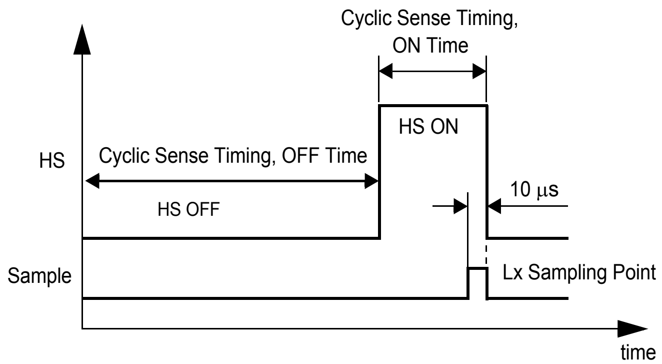


Figure 27. HS Operation When Cyclic Sense Is Selected

Table 29. TIM2 Control Bits

CSP2	CSP1	CSP0	Cyclic Sense Timing (ms)	Parameter
0	0	0	4.6	Cyclic Sense/FWU Timing 1
0	0	1	9.25	Cyclic Sense/FWU Timing 2
0	1	0	18.5	Cyclic Sense/FWU Timing 3
0	1	1	37	Cyclic Sense/FWU Timing 4
1	0	0	74	Cyclic Sense/FWU Timing 5
1	0	1	95.5	Cyclic Sense/FWU Timing 6
1	1	0	191	Cyclic Sense/FWU Timing 7
1	1	1	388	Cyclic Sense/FWU Timing 8

Low Power Control Register (LPC)

Tables 30 through 34 contain various Low Power Control Register information. The LPC register controls:

- The state of HS in Stop and Sleep modes (HS permanently OFF or HS cyclic).
- Enable or disable of the forced wake-up function (33742 automatic wake-up after time spent in Sleep or Stop modes; time is defined by the TIM2 subregister).
- Enable or disable the sense of the wake-up inputs (Lx) at the sampling point of the Cyclic Sense period (LX2HS bit). (Refer to Reset Control Register (RCR) on page 40 for details of the LPC register setup required for proper cyclic sense or direct wake-up operation.

The LPC register also reports the CANH and RXD diagnostic.

Table 30. Low Power Control Register

LPC	R/W	D3	D2	D1	D0
$110b	W	LX2HS	FWU	CAN-INT	HSAUTO
	R	CANH2VDD	CANH2BAT	CANH2GND	RXPR
Reset Value	–	0	0	0	0
Reset Condition (Write) (Note 62)	–	POR, NR2R, N2R, STB2R, STO2R	POR, NR2R, N2R, STB2R, STO2R	POR, NR2R, N2R, STB2R, STO2R	POR, NR2R, N2R, STB2R, STO2R

Notes
62. See Table 8, page 38, for definitions of reset conditions.

Table 31. LX2HS Control Bits

Value	Wake-Up Inputs Supplied by HS
0	No.
1	Yes. Lx inputs sensed at sampling point.

Table 32. HSAUTO Control Bits

Value	Auto-Timing HS in Sleep and Stop Modes
0	OFF.
1	ON, HS Cyclic, period defined in TIM2 subregister.

Table 33. CAN-INT Control Bits

Value (Note 63)	Description
0	Interrupt as soon as CAN bus failure detected.
1	Interrupt when CAN bus failure detected and fully identified.

Notes
63. If CAN-INT is at 0, any undetermined CAN failure will be latched in the CAN register (bit D1: CAN-UF) and can be accessed by SPI (refer to CAN Register (CAN) on page 40). After reading the CAN register or setting CAN-INT to 1, it will be cleared automatically. The existence of CAN-UF always has priority over clearing, meaning that a further undetermined CAN failure does not allow clearing the CAN-UF bit.

Table 34. LPC Status Bits

Name	Value	Failure Description
CANH2VDD	0	No CANH short to V_{DD}.
	1	CANH short to V_{DD}.
CANH2BAT	0	No CANH short to V_{SUP}.
	1	CANH short to V_{SUP}.
CANH2GND	0	No CANH short to GND.
	1	CANH short to GND.
RXPR	0	No RXD permanent recessive.
	1	RXD permanent recessive.

Interrupt Register (INTR)

Tables 35 through 37 contain various Interrupt Register information. The INTR register allows masking or enabling the interrupt source. A read operation identifies the interrupt source. Table 37 provides status bit information. The status bits of the INTR register content are copies of the IOR, CAN, TIM, and LPC registers status content. To clear the Interrupt Register bits, the IOR, CAN, TIM, and/or LPC registers must be cleared (read register) and the recovery condition must occur. Errors bits are latched in the CAN register and the IOR register.

Table 35. Interrupt Register

INTR	R/W	D3	D2	D1	D0
$111b	W	VSUPLOW	HSOT-V2LOW (Note 64)	VDDTEMP	CANF
	R	VSUPLOW	HSOT	VDDTEMP	CANF
Reset Value	–	0	0	0	0
Reset Condition (Write) (Note 65)	–	POR, RST	POR, RST	POR, RST	POR, RST

Notes

64. If only HSOT - V2LOW interrupt is selected (only bit D2 set in INTR register), reading INTR register bit D2 leads to two possibilities:
    1. Bit D2 = 1: Interrupt source is HSOT.
    2. Bit D2 = 0: Interrupt source is V2LOW.
    HSOT and V2LOW bits status are available in the IOR register.
65. See Table 8, page 38, for definitions of reset conditions.

Table 36. Interrupt Register Control Bits

Name	Description
CANF	Mask bit for CAN failures.
VDDTEMP	Mask bit for V_{DD} medium temperature (pre-warning).
HSOT - V2LOW	Mask bit for HS overtemperature AND V2 < 4.0 V.
VSUPLOW	Mask bit for V_{SUP} < 6.1 V.

When the mask bit is set, the $\overline{INT}$ terminal goes low if the appropriate condition occurs. Upon a wake-up condition from Stop mode due to overcurrent detection ($I_{DDS-WU1}$ or $I_{DDS-WU2}$), an $\overline{INT}$ pulse is generated; however, INTR register content remains at 0000 (not bit set into the INTR register).

Table 37. Interrupt Register Status Bits

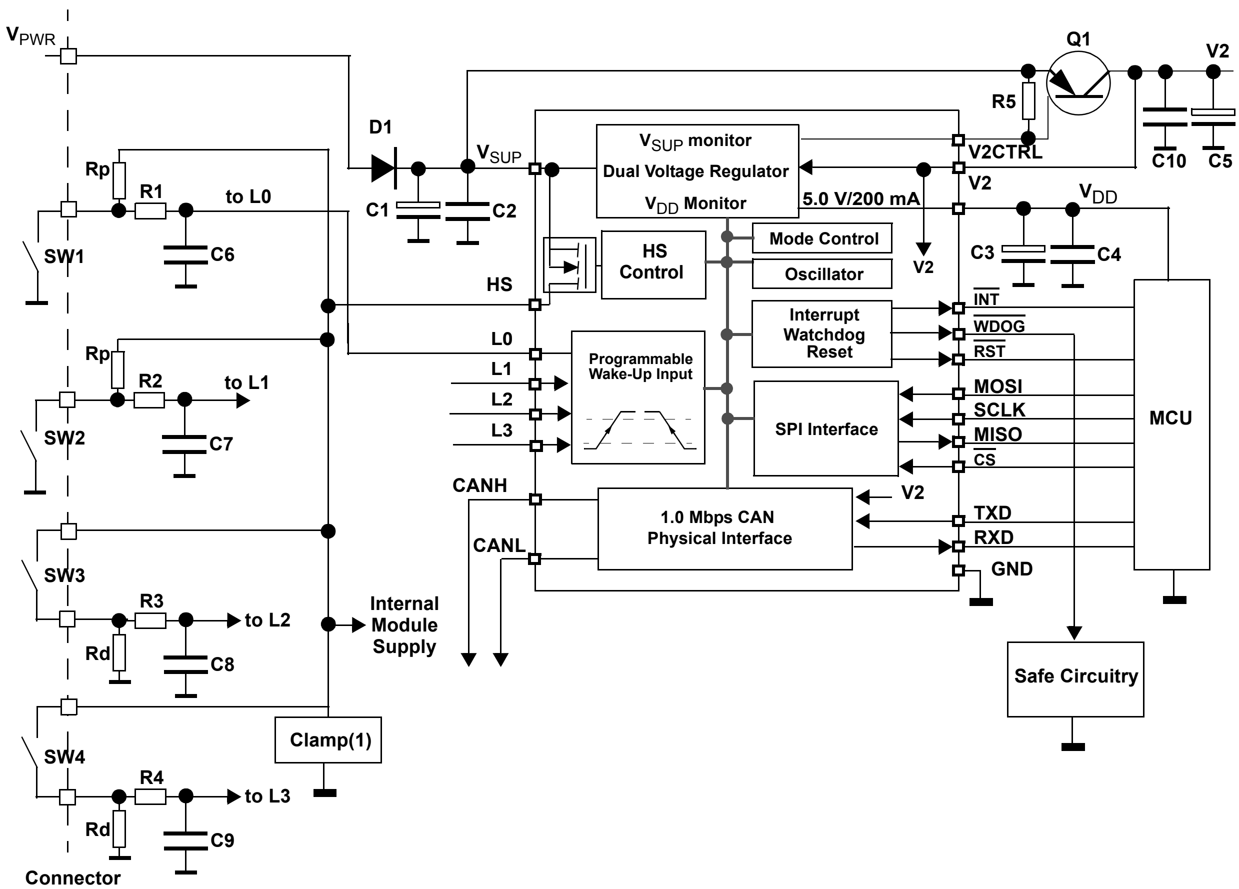
Name	Value	Description
VSUPLOW	0	No V_{SUP} < 6.1 V.
	1	V_{SUP} < 6.1 V.
HSOT	0	No HS overtemperature.
	1	HS overtemperature.
VDDTEMP	0	No V_{DD} medium temperature (pre-warning).
	1	V_{DD} medium temperature (pre-warning).
CANF	0	No CAN failure.
	1	CAN failure.

PACKAGE AND THERMAL CONSIDERATIONS

The 33742 is a standard surface mount SOIC 28 package. In order to improve the thermal performances of the SOIC 28 package, eight terminals are internally connected to the lead frame and are used for heat transfer to the printed circuit board.

APPLICATIONS

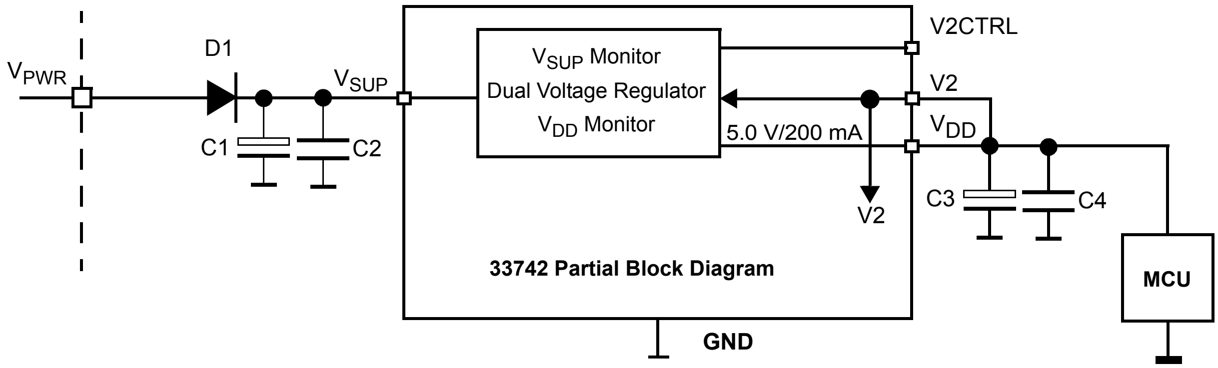
Figure 28 shows a typical 33742 application.



Legend

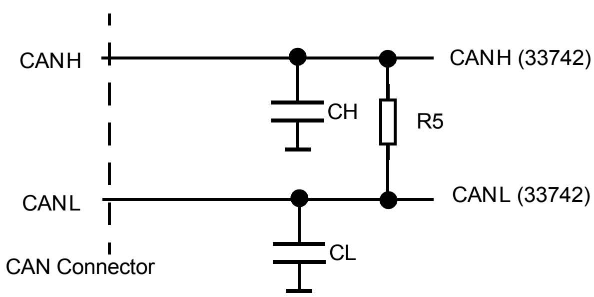
D1: Example: 1N4002 type
Q1: MJD32C
R1, R2, R3, R4: 10 kΩ
Rp, Rd: Example: 1.0 kΩ depending on switch type.
R5: 2.2 kΩ
C1: 10 µF
C2: 100 nF
C3: 47 µF
C4: 100 nF
C5: 47 µF tantalum or 100 µF chemical
C6, C7, C8, C9, C10: 100 nF
(1) Clamp circuit to ensure max ratings for HS (HS from -0.3 V to V_{SUP} + 0.3) are respected.

Figure 28. 33742 Typical Application Schematic



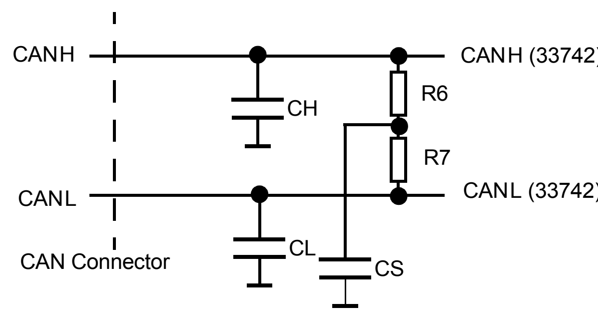
Legend
D1: Example: 1N4002 type
C1: 10 µF
C2: 100 nF
C3: 47 µF
C4: 100 nF

Figure 29. 33742 Application Without External Ballast Transistor on V2 Regulator



Legend
R5: 60 Ω
CL, CH: 220 pF

Figure 30. CAN Bus Standard Termination

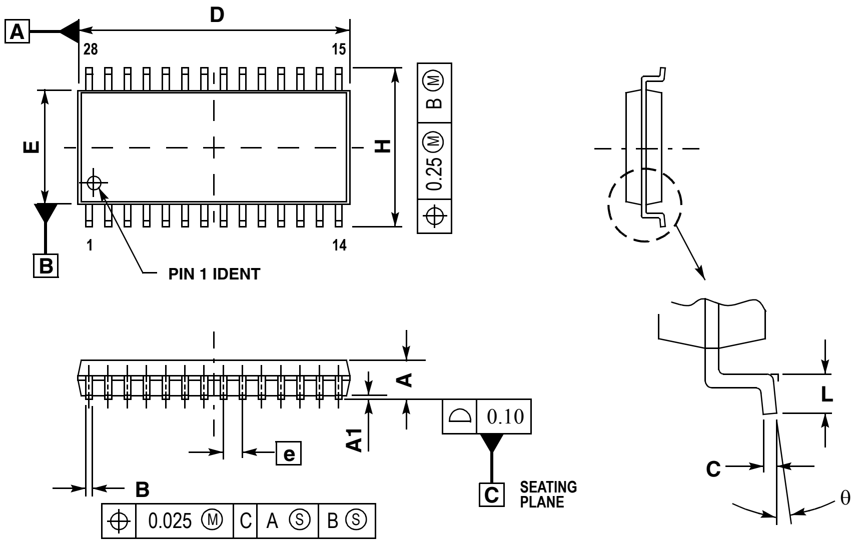


Legend
R6, R7: 30 Ω
CL, CH: 220 pF
CS: > 470 pF

Figure 31. CAN Bus Split Termination

PACKAGE DIMENSIONS

DW SUFFIX
28-LEAD SOICW
PLASTIC PACKAGE
CASE 751F-05
ISSUE F



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
4. MAXIMUM MOLD PROTRUSION 0.015 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.13	0.29
B	0.35	0.49
C	0.23	0.32
D	17.80	18.05
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
L	0.41	0.90
θ	0°	8°

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