INITIAL RELEASE

Final Electrical Specifications

LT1640L/LT1640H

Negative Voltage Hot Swap Controller

July 1998

FEATURES

- **Allows Safe Board Insertion and Removal from a Live –48V Backplane**
- **Operates from –10V to –80V**
- **Programmable Inrush Current**
- Programmable Electronic Circuit Breaker
- Programmable Overvoltage Protection
- Programmable Undervoltage Lockout
- Power Good Control Output

APPLICATIONS

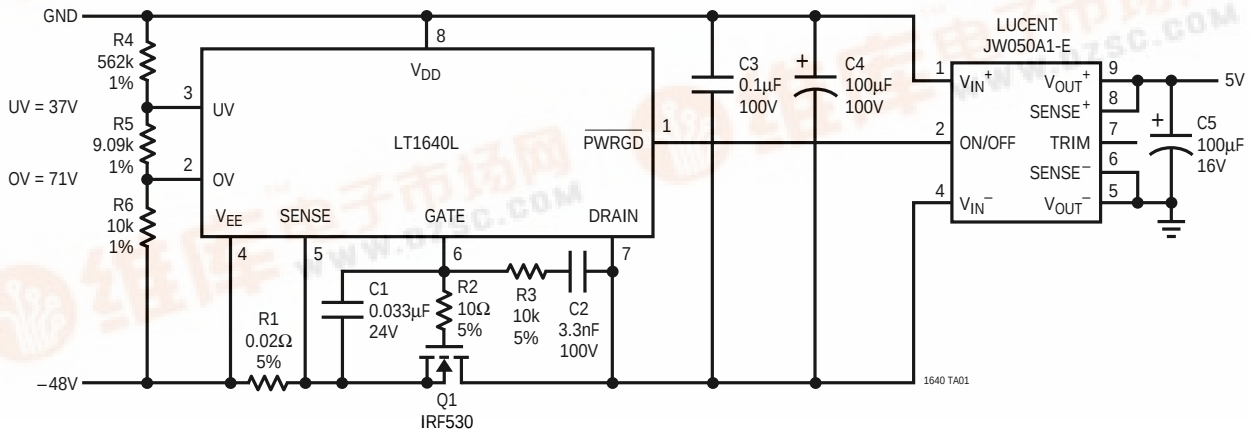
- Central Office Switching
- –48V Distributed Power Systems

DESCRIPTION

The LT®1640L/LT1640H is an 8-pin, negative voltage Hot Swap™ controller that allows a board to be safely inserted and removed from a live backplane. Inrush current is limited to a programmable value by controlling the gate voltage of an external N-channel pass transistor. The pass transistor is turned off if the input voltage is less than the programmable undervoltage threshold or greater than the overvoltage threshold. A programmable electronic circuit breaker protects the system against shorts. The PWRGD or $\overline{\text{PWRGD}}$ signal can be used to directly enable a power module. The LT1640L is designed for modules with a low enable input and the LT1640H for modules with a high enable input.

The LT1640L/LT1640H is available in 8-pin PDIP and SO packages.

TYPICAL APPLICATION

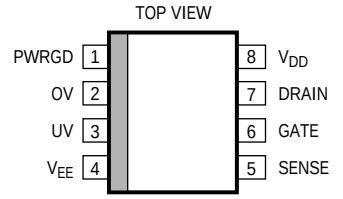


ABSOLUTE MAXIMUM RATINGS (Note 1), All Voltages Referred to V_{EE}

Supply Voltage ($V_{DD} - V_{EE}$) ..... –0.3V to 100V
DRAIN, PWRGD, $\overline{PWRGD}$ Pins ..... –0.3V to 100V
SENSE, GATE Pins ..... –0.3V to 20V
UV, OV Pins ..... –0.3V to 60V
Maximum Junction Temperature ..... 125°C

Operating Temperature Range
LT1640HC/LT1640LC ..... 0°C to 70°C
LT1640HI/LT1640LI ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

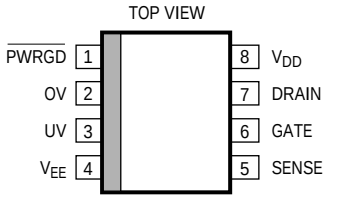
PACKAGE/ORDER INFORMATION



N8 PACKAGE 8-LEAD PDIP
S8 PACKAGE 8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 120°C/W (N8)
T_{JMAX} = 125°C, θ_{JA} = 150°C/W (S8)

ORDER PART NUMBER
LT1640HCN8 LT1640HCS8 LT1640HIN8 LT1640HIS8
S8 PART MARKING
1640H 1640HI



N8 PACKAGE 8-LEAD PDIP
S8 PACKAGE 8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 120°C/W (N8)
T_{JMAX} = 125°C, θ_{JA} = 150°C/W (S8)

ORDER PART NUMBER
LT1640LCN8 LT1640LCS8 LT1640LIN8 LT1640LIS8
S8 PART MARKING
1640L 1640LI

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS (Note 2), V_{DD} = 48V, V_{EE} = 0V, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC							
V_{DD}	Supply Voltage		●	10		80	V
I_{DD}	Supply Current	UV = 3V, OV = V_{EE}, SENSE = V_{EE}	●		2	5	mA
V_{CB}	Circuit Breaker Trip Voltage	V_{CB} = (V_{SENSE} – V_{EE})	●	40	50	60	mV
I_{PU}	GATE Pin Pull-Up Current	Gate Drive On, V_{GATE} = V_{EE}	●	–30	–45	–60	µA
I_{PD}	GATE Pin Pull-Down Current	Any Fault Condition		24	50	70	mA
ΔV_{GATE}	External Gate Drive	(V_{GATE} – V_{EE}), 15V ≤ V_{DD} ≤ 80V (V_{GATE} – V_{EE}), 10V ≤ V_{DD} < 15V	● ●	10 6	13.5 8	18 15	V V
V_{UVH}	UV Pin High Threshold Voltage	UV Low to High Transition	●	1.213	1.243	1.272	V
V_{UVL}	UV Pin Low Threshold Voltage	UV High to Low Transition	●	1.198	1.223	1.247	V
V_{UVHY}	UV Pin Hysteresis				20		mV
I_{INUV}	UV Pin Input Current	V_{UV} = V_{EE}	●		–0.02	–0.5	µA
V_{OVH}	OV Pin High Threshold Voltage	OV Low to High Transition	●	1.198	1.223	1.247	V
V_{OVL}	OV Pin Low Threshold Voltage	OV High to Low Transition	●	1.165	1.203	1.232	V
V_{OVHY}	OV Pin Hysteresis				20		mV
I_{INOV}	OV Pin Input Current	V_{OV} = V_{EE}	●		–0.03	–0.5	µA
V_{PG}	Power Good Threshold	V_{DRAIN} – V_{EE}, High to Low Transition		1.1	1.4	2.0	V
V_{PGHY}	Power Good Threshold Hysteresis				0.4		V
V_{OL}	Output Low Voltage	$\overline{PWRGD}$ (LT1640L), I_{OUT} = 1mA, (V_{DRAIN} – V_{EE}) < V_{PG}	●		0.48	0.8	V
R_{OUT}	Power Good Output Impedance	PWRGD (LT1460H), (V_{DRAIN} – V_{EE}) < V_{PG}	●	2	6.5		kΩ

ELECTRICAL CHARACTERISTICS

V_{DD} = 48V, V_{EE} = 0V, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC							
t_{PHLOV}	OV High to GATE Low	Figures 1, 2			1.7		µs
t_{PHLUV}	UV Low to GATE Low	Figures 1, 3			1.5		µs
t_{PLHOV}	OV Low to GATE High	Figures 1, 2			5.5		µs
t_{PLHUV}	UV High to GATE High	Figures 1, 3			6.5		µs
$t_{PHLSENSE}$	SENSE High to Gate Low	Figures 1, 4		2	3	4	µs
t_{PHLPG}	DRAIN Low to $\overline{PWRGD}$ Low DRAIN Low to (PWRGD – DRAIN) High	(LT1640L) Figures 1, 5 (LT1640H) Figures 1, 5			0.5 0.5		µs µs
t_{PLHPG}	DRAIN High to $\overline{PWRGD}$ High DRAIN High to (PWRGD – DRAIN) Low	(LT1640L) Figures 1, 5 (LT1640H) Figures 1, 5			0.5 0.5		µs µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

PIN FUNCTIONS

$\overline{PWRGD}$/PWRGD (Pin 1): Power Good Output Pin. This pin will toggle when V_{DRAIN} is within V_{PG} of V_{EE}. This pin can be connected directly to the enable pin of a power module.

When the DRAIN pin of the LT1640H is above V_{EE} by more than V_{PG}, the PWRGD pin will sink current to the DRAIN pin which pulls the module's enable pin low, forcing it off. When V_{DRAIN} drops below V_{PG}, the PWRGD sink current is turned off and a 5k resistor is connected between PWRGD and DRAIN, allowing the module's pull-up current to pull the enable pin high and turn on the module.

When the DRAIN pin of the LT1640L is above V_{EE} by more than V_{PG}, the $\overline{PWRGD}$ pin will be high impedance, allowing the pull-up current of the module's enable pin to pull the pin high and turn the module off. When V_{DRAIN} drops below V_{PG}, the $\overline{PWRGD}$ pin sinks current to V_{EE}, pulling the enable pin low and turning on the module.

OV (Pin 2): Analog Overvoltage Input. When OV is pulled above the 1.223V low to high threshold, an overvoltage condition is detected and the GATE pin will be immediately pulled low. The GATE pin will remain low until OV drops below the 1.203V high to low threshold.

UV (Pin 3): Analog Undervoltage Input. When UV is pulled below the 1.223V high to low threshold, an undervoltage condition is detected and the GATE pin will be immediately pulled low. The GATE pin will remain low until UV rises above the 1.243 low to high threshold.

The UV pin is also used to reset the electronic circuit breaker. If the UV pin is cycled low and high following the trip of the circuit breaker, the circuit breaker is reset and a normal power-up sequence will occur.

V_{EE} (Pin 4): Negative Supply Voltage Input. Connect to the lower potential of the power supply.

SENSE (Pin 5): Circuit Breaker Sense Pin. With a sense resistor placed in the supply path between V_{EE} and SENSE, the circuit breaker will trip when the voltage across the resistor exceeds 50mV. Noise spikes of less than 2µs are filtered out and will not trip the circuit breaker.

If the circuit breaker trip current is set to twice the normal operating current, only 25mV is dropped across the sense resistor during normal operation. To disable the circuit breaker, V_{EE} and SENSE can be shorted together.

PIN FUNCTIONS

GATE (Pin 6): Gate Drive Output for the External N-Channel. The GATE pin is allowed to go high when the following start-up conditions are met: the UV pin is high, the OV pin is low and ($V_{SENSE} – V_{EE}$) < 50mV. The GATE pin is pulled high by a 45µA current source and pulled low with a 50mA current source.

DRAIN (Pin 7): Analog Drain Sense Input. Connect this pin to the drain of the external N-channel and the V^- pin of the power module. When the DRAIN pin is below V_{PG}, the PWRGD or $\overline{PWRGD}$ pin will toggle.

V_{DD} (Pin 8): Positive Supply Voltage Input. Connect this pin to the higher potential of the power supply inputs and the V^+ pin of the power module. The input supply voltage ranges from 10V to 80V.

TEST CIRCUIT

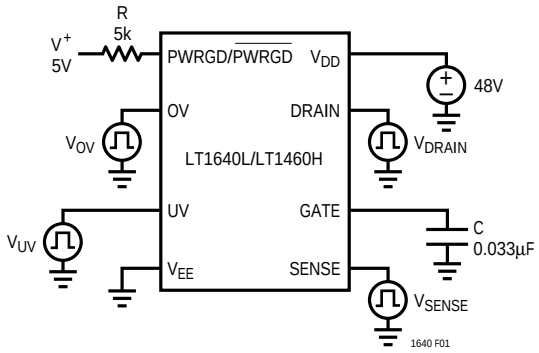


Figure 1. Test Circuit

TIMING DIAGRAMS

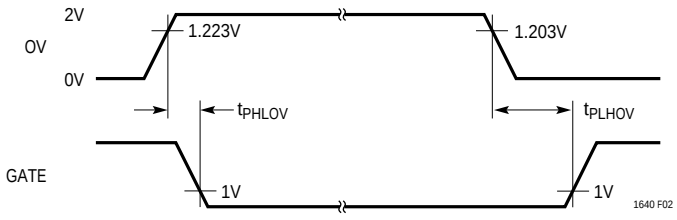


Figure 2. OV to GATE Timing

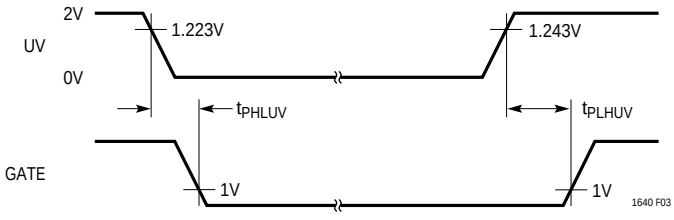


Figure 3. UV to GATE Timing

TIMING DIAGRAMS

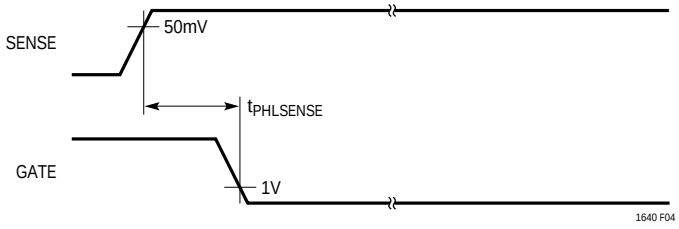


Figure 4. SENSE to GATE Timing

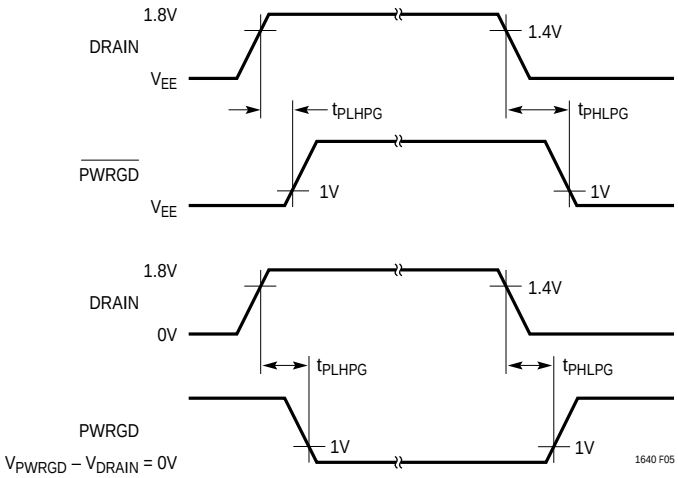


Figure 5. DRAIN to PWRGD/$\overline{\text{PWRGD}}$ Timing

APPLICATIONS INFORMATION

Hot Circuit Insertion

When circuit boards are inserted into a live –48V backplane, the bypass capacitors at the input of the board's power module or switching power supply can draw huge transient currents as they charge up. The transient currents can cause permanent damage to the board's components and cause glitches on the system power supply.

The LT1640 is designed to turn on a board's supply voltage in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. The chip also provides undervoltage, overvoltage and overcurrent protection while keeping the power module off until its input voltage is stable and within tolerance.

Power Supply Ramping

The input to the power module on a board is controlled by placing an external N-channel pass transistor (Q1) in the power path (Figure 6a, all waveforms are with respect to the V_{EE} pin of the LT1640). R1 provides current fault detection and R2 prevents high frequency oscillations. Resistors R4, R5 and R6 provide undervoltage and overvoltage sensing. By ramping the gate of Q1 up at a slow rate, the surge current charging load capacitors C3 and C4

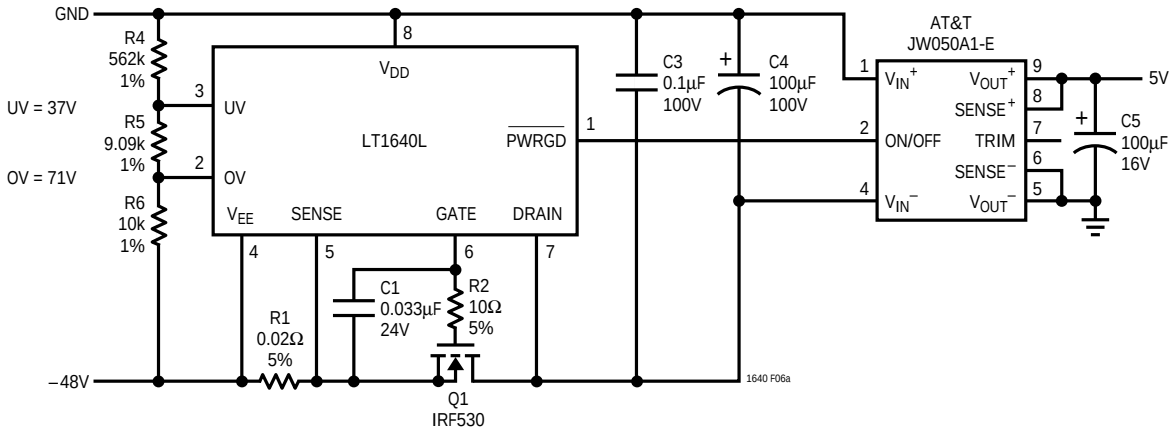


Figure 6a. Simple Inrush Control Circuitry

APPLICATIONS INFORMATION

can be limited to a safe value when the board makes connection.

The waveforms are shown in Figure 6b. When the power pins make contact, they bounce several times. The DRAIN and UV pin voltages also bounce, ramping the GATE pin at a rate set by the 45µA GATE current source and C1. When the GATE voltage reaches the threshold voltage of Q1, the DRAIN voltage ramps down and the input current spikes as C3 and C4 is charged. Because Q1 is acting as a common source amplifier, the inrush current is not well controlled but can be kept to a safe value.

An improved inrush control circuit is shown in Figure 7a. Resistor R3 and capacitor C2 act as a feedback network to accurately control the inrush current. The inrush current can be calculated with the following equation:

$$I_{INRUSH} = (45\mu A \bullet C_L)/C2$$

where C_L is the total load capacitance. Resistor R3 helps keep Q1 off when the power pins first make contact. The waveforms are shown in Figure 7b. When the power pins make contact, they bounce several times. While the contacts are bouncing, the LT1640 senses an undervoltage condition and the GATE is immediately pulled low when the power pins are disconnected.

Once the power pins stop bouncing, the GATE pin starts to ramp up. When Q1 turns on, the GATE voltage is held

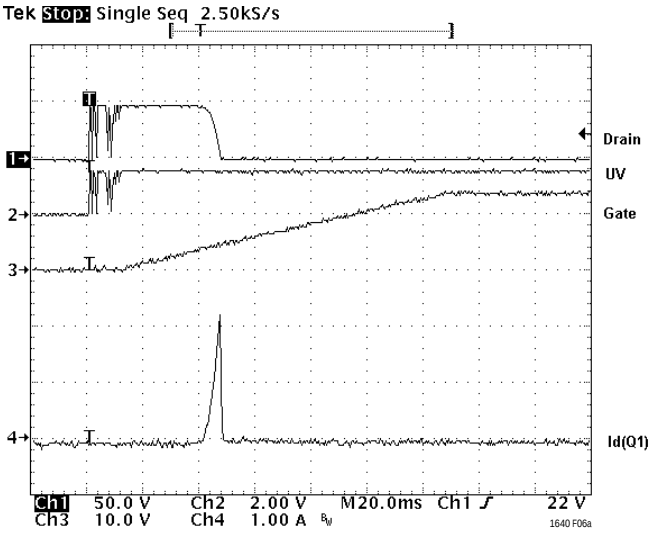


Figure 6b. Simple Inrush Control Waveforms

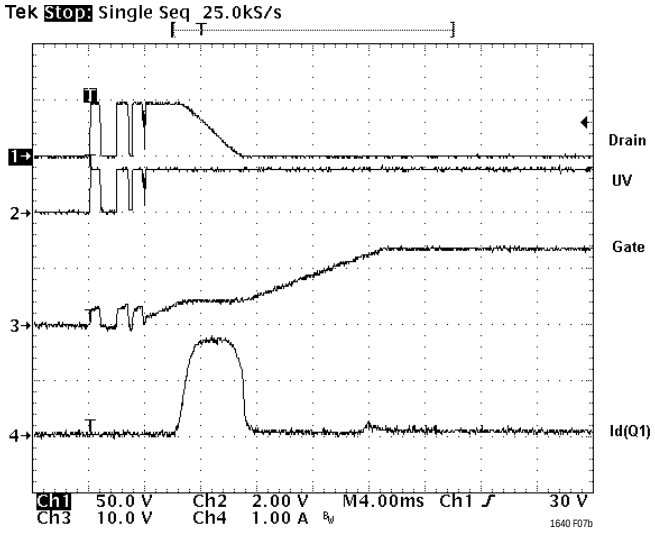


Figure 7b. Improved Inrush Control Waveforms

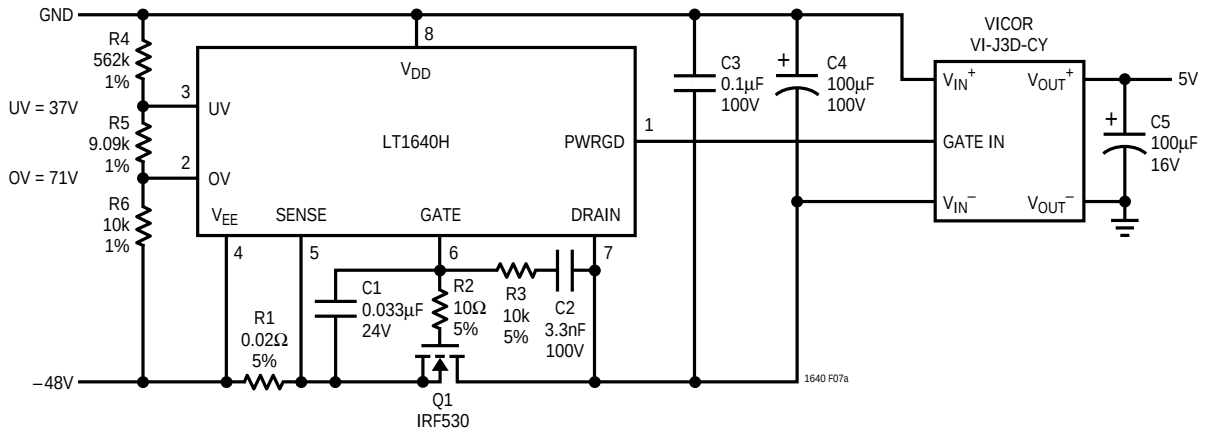


Figure 7a. Improved Inrush Control Circuitry

APPLICATIONS INFORMATION

constant by the feedback network of R3 and C2. When the DRAIN voltage has finished ramping, the GATE pin then ramps to its final value.

Electronic Circuit Breaker

The LT1640 features an electronic circuit breaker function that protects against short circuits or excessive supply currents. By placing a sense resistor between the V_{EE} and SENSE pin, the circuit breaker will be tripped whenever the voltage across the sense resistor is greater than 50mV for more than 3µs as shown in Figure 8.

When the circuit breaker trips, the GATE pin is immediately pulled to V_{EE} and the external N-channel turns off. The GATE pin will remain low until the circuit breaker is reset by pulling UV low, then high or cycling power to the part.

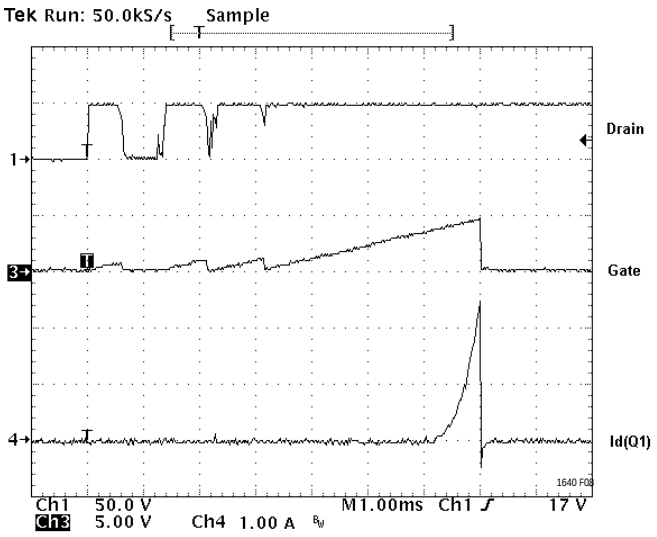


Figure 8. Short-Circuit Protection Waveforms

If more than 3µs deglitching time is needed to reject current noise, an external resistor and capacitor can be added to the sense circuit as shown in Figure 9. If the circuit breaker feature is not required, the SENSE pin should be shorted to V_{EE}.

A circuit that automatically resets the circuit breaker after a current fault is shown in Figure 10.

Transistors Q2 and Q3 along with R7, R8, C4 and D1 form a programmable one-shot circuit. Before a short occurs, the GATE pin is pulled high and Q3 is turned on, pulling node 2 to V_{EE}. Resistor R8 turns off Q2. When a short occurs, the GATE pin is pulled low and Q3 turns off. Node 2 starts to charge C4 and Q2 turns on, pulling the UV pin low and resetting the circuit breaker. As soon as C4 is fully charged, R8 turns off Q2, UV goes high and the GATE starts to ramp up. Q3 turns back on and quickly pulls node 2 back to V_{EE}. Diode D1 clamps node 3 one diode drop below V_{EE}. The duty cycle is set to 10% to prevent Q1 from overheating.

Undervoltage and Overvoltage Detection

The UV (Pin 3) and OV (Pin 2) pins can be used to detect undervoltage and overvoltage conditions at the power supply input. The UV and OV pins are internally connected to analog comparators with 20mV of hysteresis. When the UV pin falls below its threshold or the OV pin rises above its threshold, the GATE pin is immediately pulled low. The GATE pin will be held low until UV is high and OV is low.

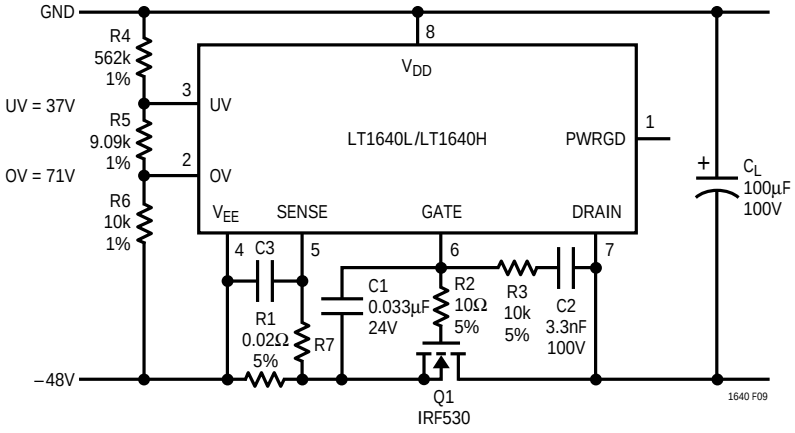
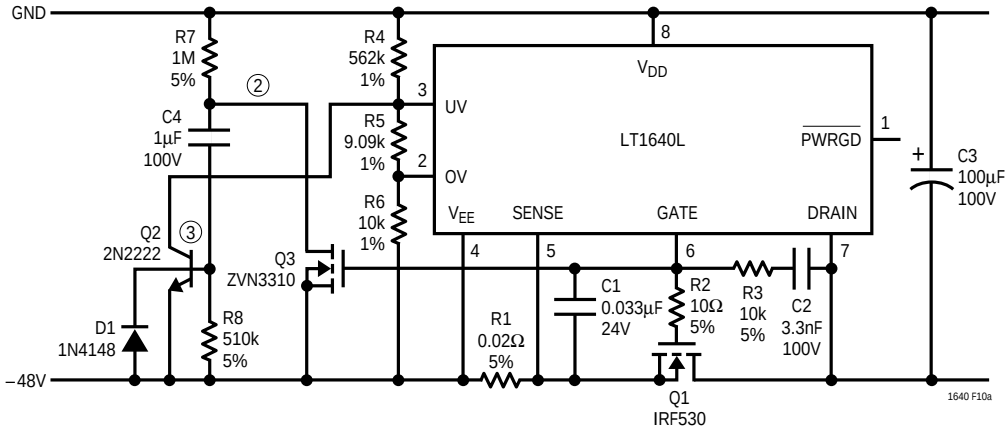


Figure 9. Extending the Short-Circuit Protection Delay

APPLICATIONS INFORMATION



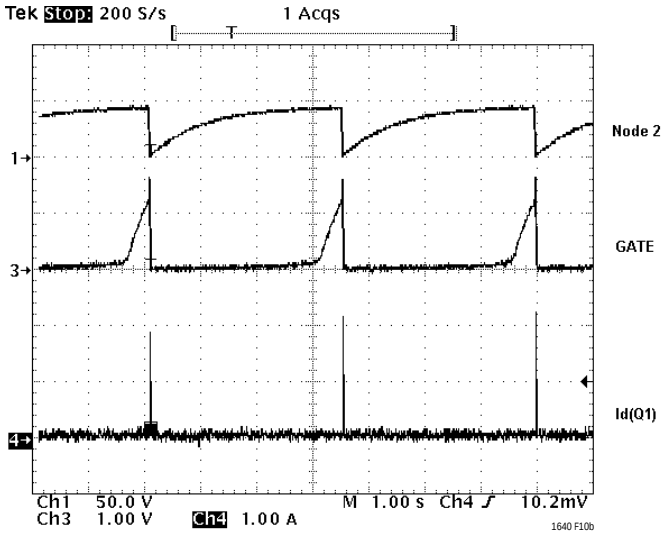


Figure 10. Automatic Restart After Current Fault

The undervoltage and overvoltage trip voltages can be programmed using a three resistor divider as shown in Figure 11. With R4 = 562k, R5 = 9.09k and R6 = 10K, the undervoltage threshold is set to 37V and the overvoltage threshold is set to 71V.

PWRGD/$\overline{\text{PWRGD}}$ Output

The PWRGD/$\overline{\text{PWRGD}}$ output can be used to directly enable a power module when the input voltage to the module is within tolerance. The LT1640H has a PWRGD output for modules with an active high enable input, and the LT1640L has a $\overline{\text{PWRGD}}$ output for modules with an active low enable input.

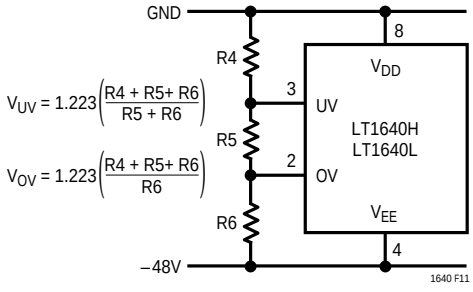


Figure 11. Undervoltage and Overvoltage Sensing

APPLICATIONS INFORMATION

When the DRAIN voltage of the LT1640H is high with respect to V_{EE} (Figure 12), the internal transistor Q3 is turned off and R7 and Q2 clamp the PWRGD pin one diode drop (≈0.7V) above the DRAIN pin. Transistor Q2 sinks the module's pull-up current and the module turns off.

When the DRAIN voltage drops below V_{PG}, Q3 will turn on, shorting the bottom of R7 to V_{EE} and turning Q2 off. The pull-up current in the module then flows through R7, pulling the PWRGD pin high and enabling the module.

When the DRAIN voltage of the LT1640L is high with respect to V_{EE}, the internal pull-down transistor Q2 is off and the $\overline{\text{PWRGD}}$ pin is in a high impedance state (Figure 13). The $\overline{\text{PWRGD}}$ pin will be pulled high by the module's internal pull-up current source, turning the module off. When the DRAIN voltage drops below V_{PG}, Q2 will turn on and the $\overline{\text{PWRGD}}$ pin will pull low, enabling the module.

The $\overline{\text{PWRGD}}$ signal can also be used to turn on an LED or optoisolator to indicate that the power is good as shown in Figure 14.

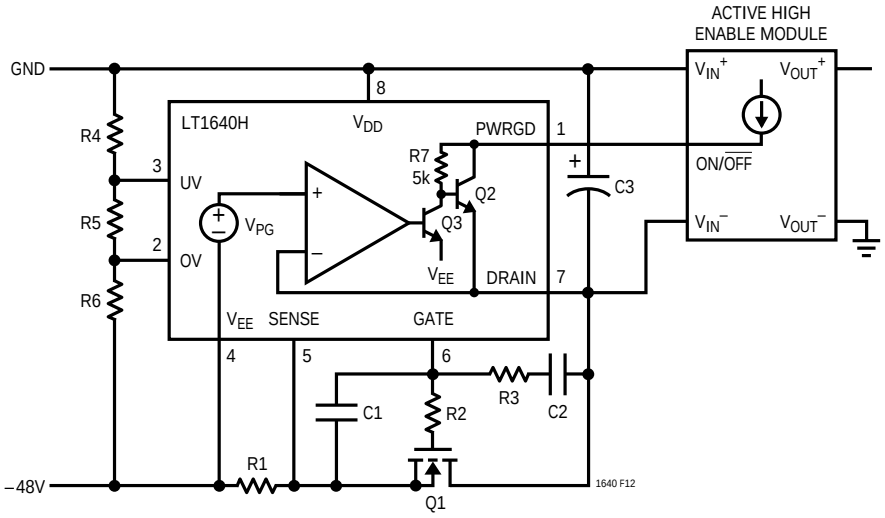


Figure 12. Active High Enable Module

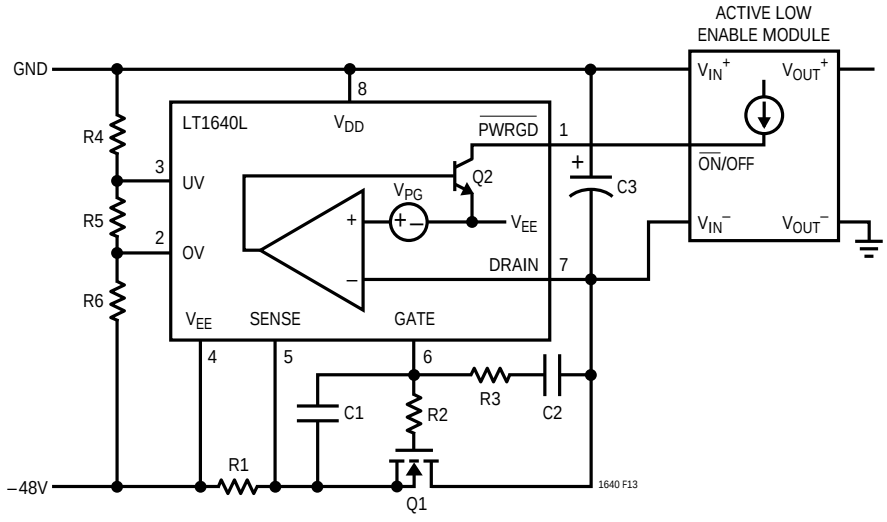


Figure 13. Active Low Enable Module

APPLICATIONS INFORMATION

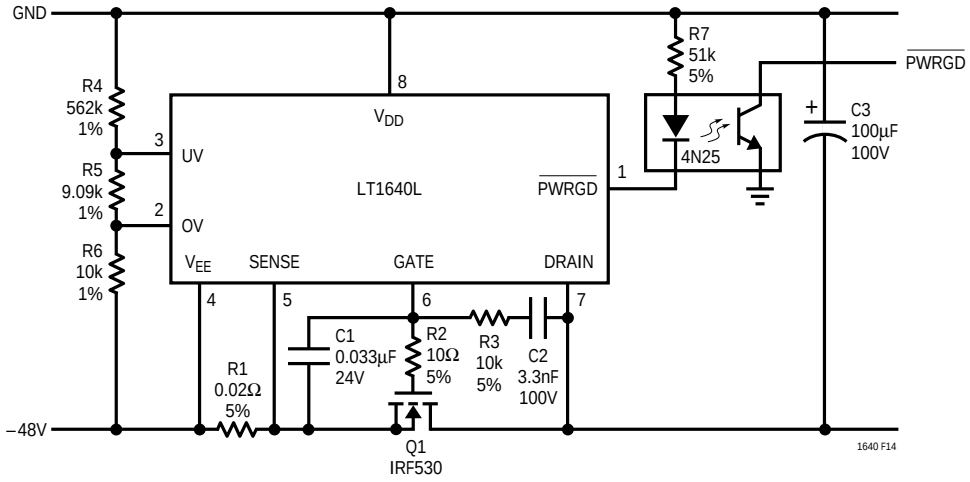


Figure 14. Using $\overline{\text{PWRGD}}$ to Drive an Optoisolator

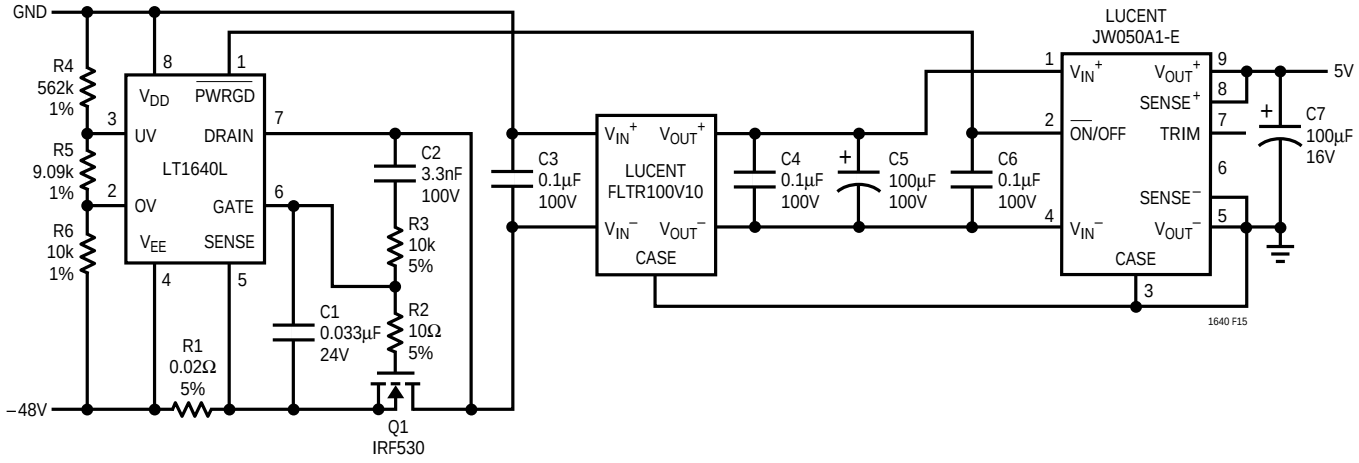


Figure 15. Typical Application Using a Filter Module

Using an EMI Filter Module

Many applications place an EMI filter module in the power path to prevent switching noise of the module from being injected back onto the power supply. A typical application using the Lucent FLTR100V10 filter module is shown in Figure 15. When using a filter, a capacitor (C6) is required across the enable pin and V_{IN}^- pin of the module to prevent noise from momentarily disabling the module.

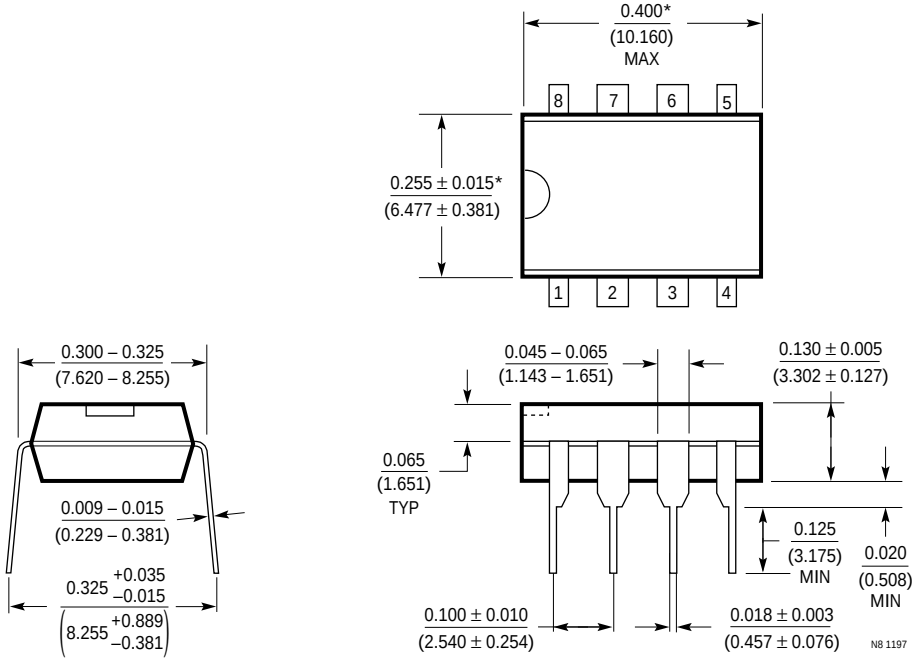
Gate Pin Voltage Regulation

When the supply voltage to the chip is more than 15.5V, the GATE pin voltage is regulated at 13.5V above V_{EE}. If the supply voltage is less than 15.5V, the GATE voltage will be about 2V below the supply voltage. At the minimum 10V supply voltage, the gate voltage is guaranteed to be greater than 6V. The gate voltage will be no greater than 18V for supply voltages up to 80V.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

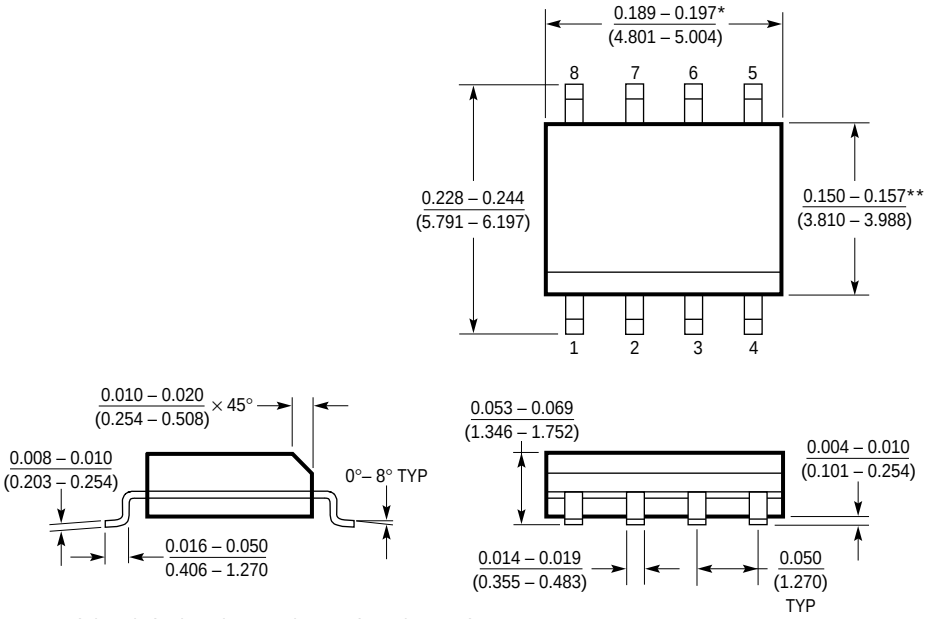


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SO8 0996

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC®1421	Two Channels, Hot Swap Controller	Operates from 3V to 12V
LTC1422	High Side Drive, Hot Swap Controller in SO-8	System Reset Output with Programmable Delay