# CH7023/CH7024 TV Encoder

## Features

- TV encoder targeting handheld and similar systems
- Support for NTSC, PAL
- Video output support for CVBS or S-video
- Macrovision™ 7.1.L1 copy protection support for SDTV (CH7023 only)
- Programmable 24-bit/18-bit/16-bit/15-bit/12-bit/8-bit digital input interface supporting various RGB and YCrCb (e.g. RGB565, RGB666, RGB888, ITU656 like YCrCb, etc.) input data formats
- Support for input resolutions up to 720x480 and 720x576 (e.g. 220x176, 320x240, 640x480, 720x480, 720x576, etc.)
- Adjustable brightness, contrast, hue and saturation.
- Detect TV / Monitor connection
- Two high quality10-bit video DAC outputs
- Fully programmable through serial port
- Flexible pixel clock frequency from graphics controller (2.3MHz—64MHz)
- Flexible input clock on the crystal or oscillator (2.3MHz—64MHz)
- Flexible up and down scaling on the display
- Master and slave mode
- Offered in 48-pin LQFP and 49-pin TFBGA Package
- IO voltage and SPC/SPD from 1.2V to 3.3V
- Programmable power management
- Power down current less than 20uA typical
- Power consumption of <150mW for one CVBS output, single terminated and <350mW for two DAC outputs, double terminated.

## General Description

The CH7023/CH7024 is a TV encoder device targeting handheld, portable video applications such as digital still cameras and similar portable embedded systems. The device is able to encode the video signals and generate synchronization signals for NTSC and PAL standards.

Supported TV output formats are NTSC-M, NTSC-J, NTSC-433, PAL-B/D/G/A/I, PAL-M, PAL-N and PAL-60.

The device accepts different data formats including RGB and YCrCb (e.g. RGB565, RGB666, RGB888, ITU656 like YCrCb, etc.) via 24 bit/18 bit/15 bit /12 bit /8 bit multiplexed digital inputs. Most embedded controllers are supported. The I/O interface voltage between CH7023/CH7024 and digital video source controller can be selected by the I/O supply voltage (VDDIO). The I/O supply voltage range is from 1.2V to 3.3V. The digital input voltage will follow the I/O supply voltage.

CH7023/CH7024 is offered in both 48-pin LQFP package (7 x 7 mm) and 49-pin TFBGA package (6 x 6 mm). CH7023/CH7024 48-pin LQFP package comes with fixed single serial port address while 49-pin TFBGA package provide two user selectable serial port addresses via AS pin pull up or pull down option. Refer to application note AN-98 for more information.

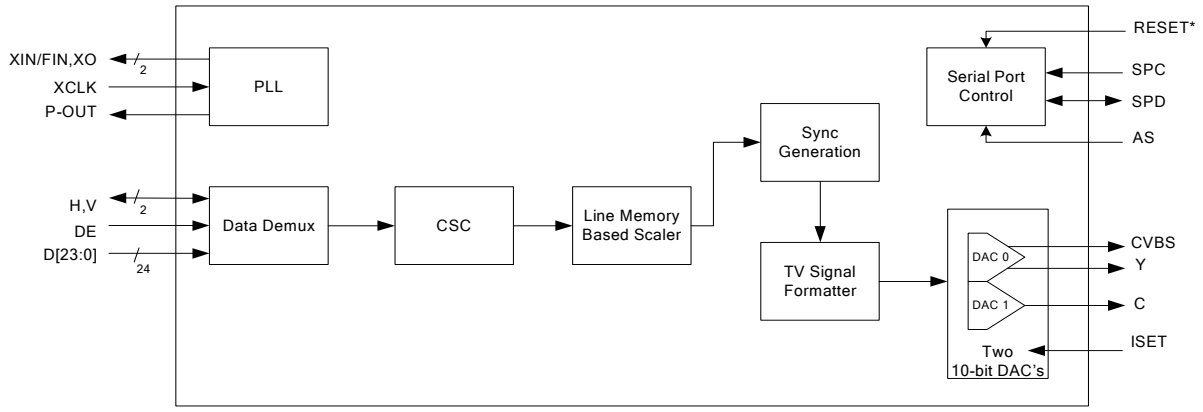


**Figure 1: CH7023/CH7024 Block Diagram**

# 1.0 PIN-OUT

There are two major differences between CH7023/CH7024 48-pin LQFP and 49-pin TFBGA in pin-out: the video DACs output and the serial port address option using AS pin.

The CH7023/CH7024 48-pin LQFP comes with three video output pins, primary CVBS (pin 28), S-video Y (pin 27) and secondary CVBS or S-video C (pin 26). The CH7023/CH7024 49-pin TFBGA comes with two video outputs, primary CVBS or S-video Y (pin E5) and secondary CVBS or S-video C (pin F6).

The CH7023/CH7024 48-pin LQFP package comes with fixed single serial port address (76h – 7 bit address) while the CH7023/CH7024 49-pin TFBGA package provides two user selectable serial port addresses via AS pin pull up or pull down option.

## 1.1 Package Diagram

### 1.1.1 The 48-pin LQFP Package Diagram

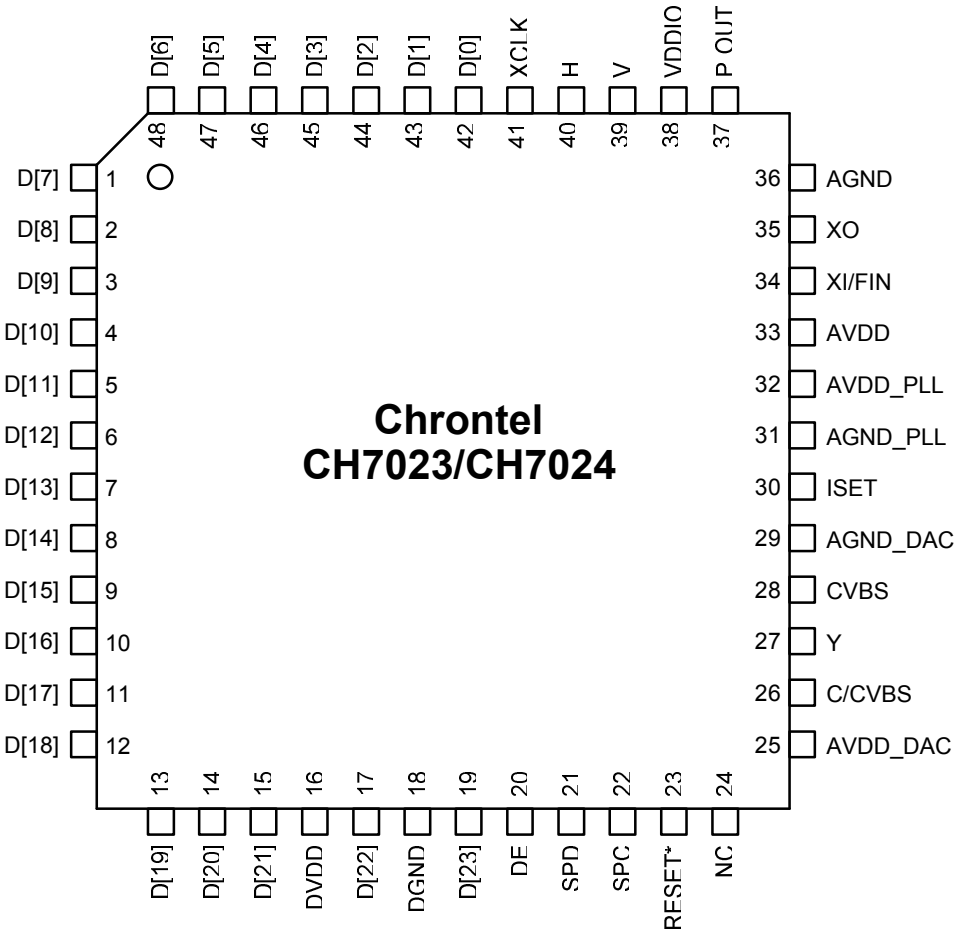


**Figure 2**: **48-LQFP Package (top view)**

### 1.1.2 The 49-pin TFBGA Package Diagram

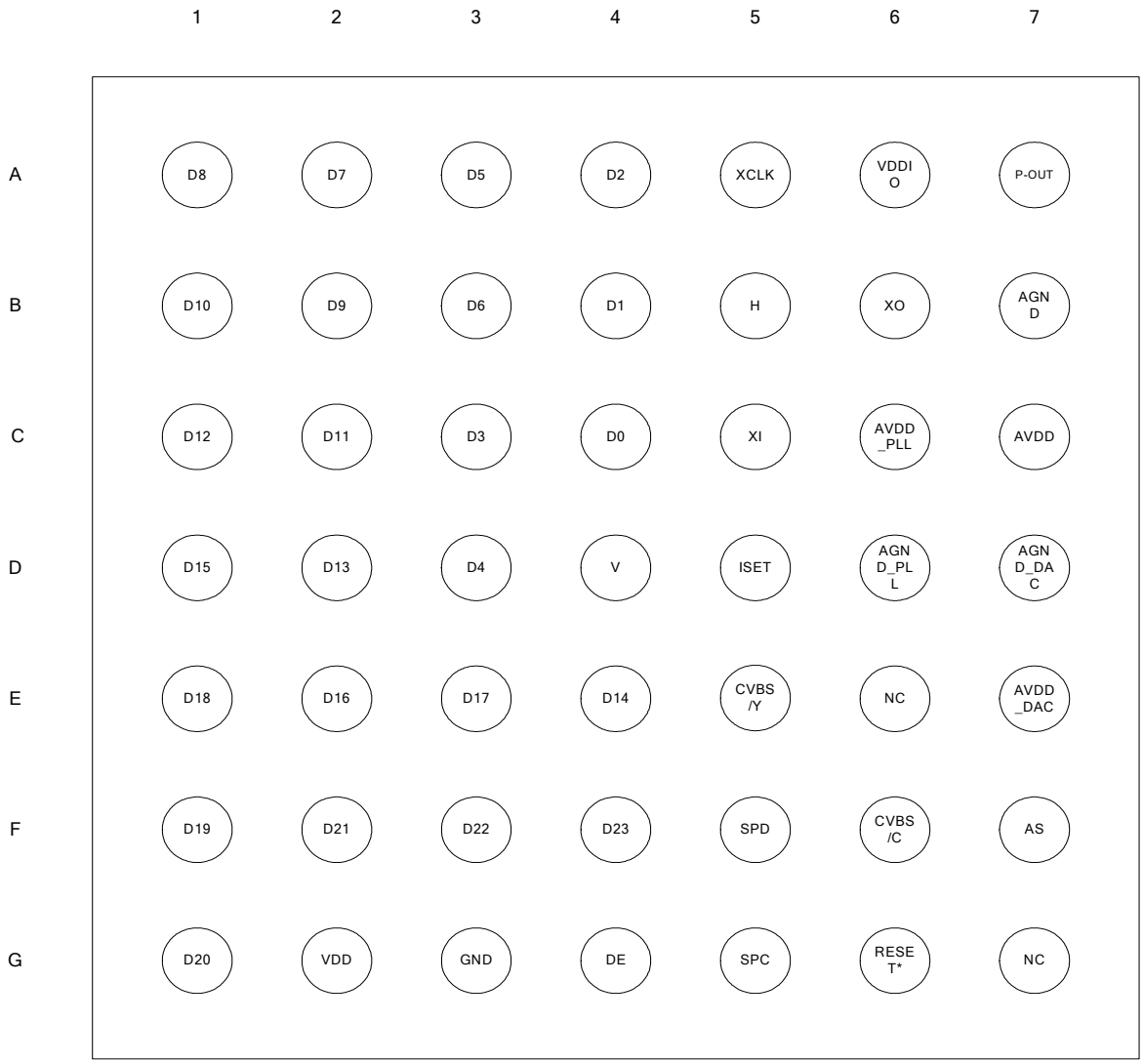


**Figure 3: 49-Pin TFBGA Package (top view)**

## 1.2 Pin Description

### 1.2.1 The 48-pin LQFP Pin Description

The 48-pin LQFP Package does not have AS pin to select second serial port address option. Refer to application note AN-98 for device address byte (DAB) details. The serial port device address for the read and write operation is fixed at ECh and EDh respectively.

It has internal switch to provide separate primary CVBS (pin 28) and S-video Y (pin27) outputs. Refer to section 2.3.2 Video DAC output and the Control Register 0Ah for the video DAC output control.

**Table 1: Pin Description (48-pin LQFP)**

| Pin # | Type | Symbol | Description |
|---|---|---|---|
| 42-48,<br>1-15,<br>17,19 | In | D[0]-D[23] | Data[0] through Data[23] Inputs<br>These pins accept 24 data input lines from a digital video port of a graphics controller. The swing is defined by VDDIO. |
| 40 | In/Out | H | Horizontal Sync Input / Output<br>When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO.<br><br>When the SYO control bit is high, the device will output a horizontal sync pulse. The amplitude will be 0 to VDDIO. |
| 39 | In/Out | V | Vertical Sync Input / Output<br>When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO.<br><br>When the SYO control bit is high, the device will output a vertical sync pulse. The amplitude will be 0 to VDDIO. |
| 20 | In | DE | Data Enable<br>When the pin is high, the input data is active.<br>When the pin is low, the input data is blanking. |
| 24 | – | NC | – |
| 23 | In | RESET* | Reset * Input<br>This pin is internally pulled high.<br>When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port. |
| 21 | In/Out | SPD | Serial Port Data Input / Output<br>This pin functions as the bi-directional data pin of the serial port and operates with input level from 0 to VDDIO. Outputs are driven from 0 to VDDIO. |
| 22 | In | SPC | Serial Port Clock Input<br>This pin functions as the clock pin of the serial port and operates with input level from 0 to VDDIO. |
| 28 | Out | CVBS | Composite Video<br>This is a primary composite vide output when S-video Y (pin 27) is not used. This output is turned off when S-video Y output is used. |
| 27 | Out | Y | Luma Output<br>The output is S-video luminance when the primary CVBS output (pin 28) is not used. |

**Table 1: Pin Description (cont'd)**

| Pin # | Type | Symbol | Description |
|---|---|---|---|
| 26 | Out | C/CVBS | Chroma/CVBS Output<br>The output is S-video chrominance when S-video is used.<br>But, when dual CVBS outputs are needed, this out pin can be used for secondary CVBS output in addition to the primary CVBS output (pin 28). |
| 30 | In | ISET | Current Set Resistor<br>This pin sets the DAC current. A 1.2k ohm, 1% tolerance resistor should be connected between this pin and AGND_DAC (pin 29) using short and wide traces. |
| 37 | Out | P-Out | Pixel Clock Output<br>This pin provides a clock signal to the graphics controller, which can be used as a reference frequency. The output driver is driven from the VDDIO supply. This output has a programmable tri-state. The capacitive loading on this pin should be kept to a minimum. |
| 34 | In | XI/FIN | Crystal Input / External Reference Input<br>For master mode and some situation of the slave mode, a parallel resonance crystal (±20 ppm) should be attached between this pin and XO. However, an external 3.3V CMOS compatible clock can drive the XI/FIN input. |
| 35 | Out | XO | Crystal Output<br>For master mode and some situation of the slave mode, a parallel resonance crystal (±20 ppm) should be attached between this pin and XI/FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open. |
| 41 | In | XCLK | External Clock Inputs<br>The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data. |
| 38 | Power | VDDIO | IO Supply Voltage (1.2-3.3V) |
| 16 | Power | DVDD | Digital Supply Voltage (1.8V) |
| 18 | Power | DGND | Digital Ground |
| 25 | Power | AVDD_DAC | DAC Supply Voltage (2.5-3.3V) |
| 29 | Power | AGND_DAC | DAC Ground |
| 32 | Power | AVDD_PLL | PLL Supply Voltage (1.8V) |
| 31 | Power | AGND_PLL | PLL Ground |
| 33 | Power | AVDD | Crystal Supply Voltage (2.5-3.3V) |
| 36 | Power | AGND | Crystal Ground |

### 1.2.2 The 49-pin TFBGA Pin Description

The 49-pin TFBGA Package has AS pin to select second serial port address. Refer to application note AN-98 for device address byte (DAB). The device address for read operation can be either ECh or EAh based on external pull-down or pull-up with AS pin respectively. The device address for write operation can be either EDh or EBh.
It does not has internal switch to provide separate primary CVBS and S-video Y outputs. Instead, it has single or dual CVBSs or S-video C and Y output. Refer to section 2.3.2 Video DAC output and the Control Register 0Ah for the video DAC output control.

**Table 2: Pin Description (49-pin TFBGA)**

| BGA Pin # | Type | Symbol | Description |
|---|---|---|---|
| A1-4,B1-B4,C1-C4,D1-D3,E1-E4, F1-F4,G1 | In | D[0]-D[23] | Data[0] through Data[23] Inputs<br>These pins accept 24 data input lines from a digital video port of a graphics controller. The swing is defined by VDDIO. |
| B5 | In/Out | H | Horizontal Sync Input / Output<br>When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDIO.<br><br>When the SYO control bit is high, the device will output a horizontal sync pulse. The output is driven from the VDDIO supply. |
| D4 | In/Out | V | Vertical Sync Input / Output<br>When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDIO.<br><br>When the SYO control bit is high, the device will output a vertical sync pulse. The output is driven from the VDDIO supply. |
| G4 | In | DE | Data Enable<br>When the pin is high, the input data is active.<br>When the pin is low, the input data is blanking. |
| F7 | In | AS | Serial Port Address Select<br>This pin is internally pulled low.<br>When AS is high, the address is 75h – 7 bit address.<br>Otherwise, the address is 76h – 7 bit address. |
| G7 | – | NC | – |
| G6 | In | RESET* | Reset * Input<br>This pin is internally pulled high.<br>When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port. |
| F5 | In/Out | SPD | Serial Port Data Input / Output<br>This pin functions as the bi-directional data pin of the serial port and operates with input level from 0 to VDDIO. Outputs are driven from 0 to VDDIO. |
| G5 | In | SPC | Serial Port Clock Input<br>This pin functions as the clock pin of the serial port and operates with input level from 0 to VDDIO. |
| E6 | – | NC | – |
| E5 | Out | CVBS/Y | Luma Output<br>The output can be either a primary CVBS or S-video luminance. |

**Table 2: Pin Description (cont'd)**

| BGA Pin # | Type | Symbol | Description |
|---|---|---|---|
| F6 | Out | CVBS/C | Chroma Output<br>The output can be either secondary CVBS when dual CVBSs are needed or S-video chrominance when S-video is selected. In single CVBS output mode, this output is turned off to save power. |
| D5 | Out | ISET | Current Set Resistor<br>This pin sets the DAC current. A 1.2k ohm, 1% tolerance resistor should be connected between this pin and AGND_DAC (pin D7) using short and wide traces. |
| A7 | Out | P-Out | Pixel Clock Output<br>This pin provides a clock signal to the graphics controller, which can be used as a reference frequency. The output driver is driven from the VDDIO supply. This output has a programmable tri-state. The capacitive loading on this pin should be kept to a minimum. |
| C5 | In | XI/FIN | Crystal Input / External Reference Input<br>For master mode and some situation of the slave mode, a parallel resonance crystal (±20 ppm) should be attached between this pin and XO. However, an external +3.3V CMOS compatible clock can drive the XI/FIN input. |
| B6 | Out | XO | Crystal Output<br>For master mode and some situation of the slave mode, a parallel resonance crystal (±20 ppm) should be attached between this pin and XI/FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open. |
| A5 | In | XCLK | External Clock Inputs<br>The input is the clock signal input to the device for use with the H, V, DE and D[23:0] data. |
| A6 | Power | VDDIO | IO Supply Voltage (1.2-3.3V) |
| G2 | Power | VDD | Digital Supply Voltage (1.8V) |
| G3 | Power | GND | Digital Ground |
| E7 | Power | AVDD_DAC | DAC Supply Voltage (2.5-3.3V) |
| D7 | Power | AGND_DAC | DAC Ground |
| C6 | Power | AVDD_PLL | PLL Supply Voltage (1.8V) |
| D6 | Power | AGND_PLL | PLL Ground |
| C7 | Power | AVDD | Crystal Supply Voltage (2.5-3.3V) |
| B7 | Power | AGND | Crystal Ground |

## 2.0 PACKAGE DIMENSIONS

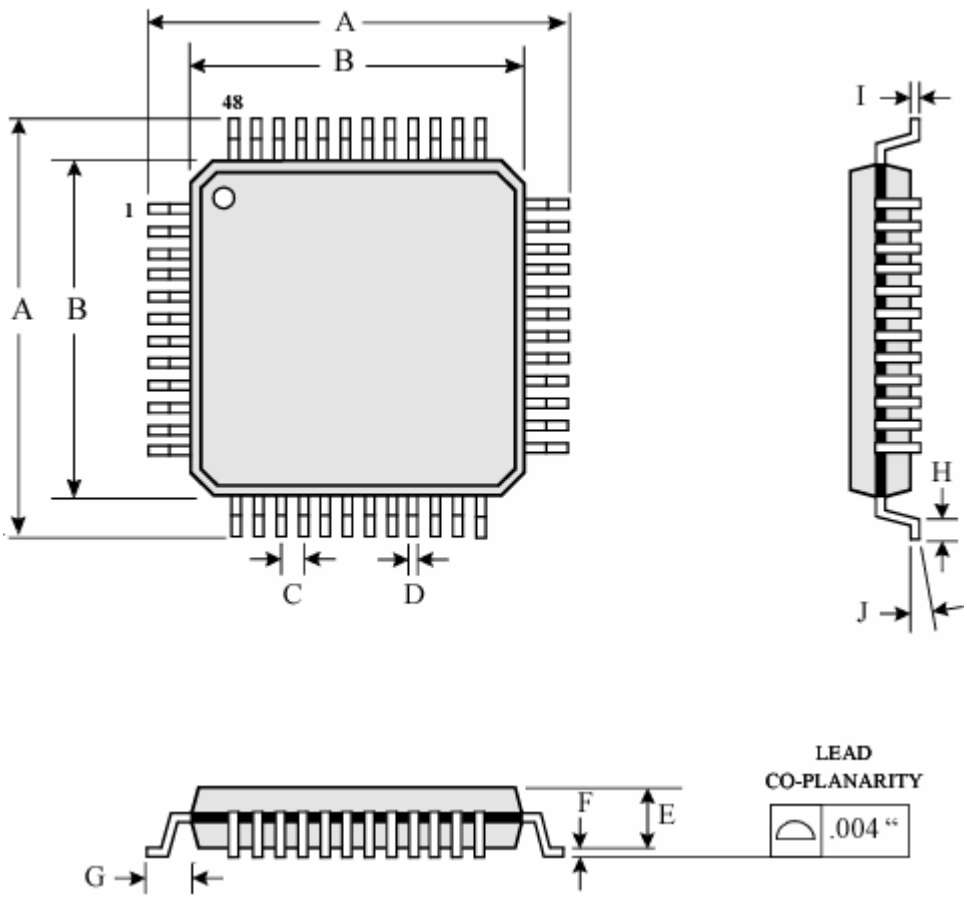


**Figure 4: 48 Pin LQFP Package**

**Table of Dimensions**

| No. of Leads | | SYMBOL | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 48 (7 X 7 mm) | | A | B | C | D | E | F | G | H | I | J |
| Milli-meters | MIN | 9 | 7 | 0.5 | 0.17 | 1.35 | 0.05 | 1.00 | 0.45 | 0.09 | 0° |
| | MAX | | | | 0.27 | 1.45 | 0.15 | | 0.75 | 0.20 | 7° |

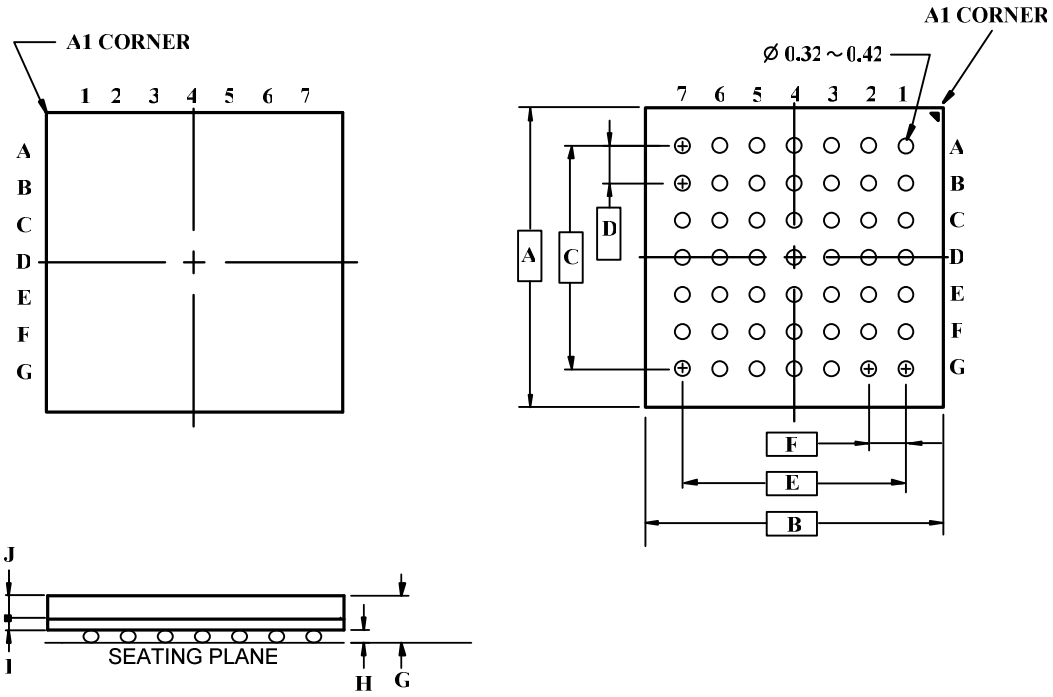


**Figure 5: 49 Pin TFBGA Package**

## Table of Dimensions

| No. of Leads | | SYMBOL | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 49 (6 X 6 mm) | | A | B | C | D | E | F | G | H | I | J |
| Milli-meters | MIN | 6.00 | 6.00 | 4.80 | 0.80 | 4.80 | 0.80 | | 0.22 | 0.26 | 0.53 |
| | MAX | | | | | | | 1.20 | 0.32 | | |

**Notes:**

1. All dimensions conform to JEDEC standard MO-216.

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**ORDERING INFORMATION**

| Part Number | Package Type | Copy Protection | Output Video Switch | Shipping Format |
|---|---|---|---|---|
| CH7023B-GF | 49TFBGA, Lead-free | Macrovision™ | No | Tray, 4290 per dry pack bag |
| CH7023B-GF-TR | 49TFBGA, Lead-free, Tape & reel | Macrovision™ | No | T&R, 2000 per dry pack bag |
| CH7023B-DF | 48LQFP, Lead-free | Macrovision™ | Yes | Tray, 2500 per dry pack bag |
| CH7023B-DF-TR | 48LQFP, Lead-free, Tape & reel | Macrovision™ | Yes | T&R, 1000 per dry pack bag |
| CH7024B-GF | 49TFBGA, Lead-free | None | No | Tray, 4290 per dry pack bag |
| CH7024B-GF-TR | 49TFBGA, Lead-free, Tape & reel | None | No | T&R, 2000 per dry pack bag |
| CH7024B-DF | 48LQFP, Lead-free | None | Yes | Tray, 2500 per dry pack bag |
| CH7024B-DF-TR | 48LQFP, Lead-free, Tape & reel | None | Yes | T&R, 1000 per dry pack bag |

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